TTL MacroFunctions
Version 1.2
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Changes are made periodically to the information contained in this manual. These changes will be incorporated into subsequent editions.

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Read This First...

Your Altera TTL MacroFunctions documentation consists of two main parts:

Introduction provides a functional description, general information on TTL MacroFunctions, and a table grouping all available TTL MacroFunctions according to their functions.

Reference Section describes in detail all presently available TTL MacroFunctions.

At the back of the manual, you find a *Customer Comment Form* and a *Problem Report Card.*

Manual Updates

Altera documentation is updated with Change Pages, Section Reprints, and a **READ.ME** file.

Change Pages are issued for minor changes to the manual. New information is identified with vertical change bars in the margins next to the changed text. In addition, the date of issue is printed at the bottom of each page.

Section Reprints are issued if a section requires a substantial number of changes. The date of issue is indicated at the bottom of each page.

A **READ.ME File** is provided on the LogiCaps **INSTALL** diskette. This file contains information about recent changes to the software that are not yet reflected in the manual.

Printing Conventions

The following notational conventiona are used throughout this manual:

Times Bold	—	all A+PLUS commands, prompts, and messages
	—	all user input, including keyboard keys
Times Light	—	most file output as displayed on screen
Helvetica Italics Bold	—	all references to Altera manual titles
Helevetica Italics Light	—	all references to sections within Altera manuals
	—	information that requires special attention

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SECTION 1

Introduction

This reference manual provides general information about the Altera TTL MacroFunction Library features and a detailed description of each TTL MacroFunction available in this library.

For detailed information on how to use this library, refer to *MacroFunction Tutorial* in the ***LogiCaps*** manual.

Functional Description

Altera's TTL MacroFunction Library is a collection of high-level building blocks, which may be used together with the gate and flipflop primitives available in the Altera Primitive Library.

The Altera Design Processor (ADP) ensures that use of TTL MacroFunctions does not cause any loss of design efficiency. It analyzes the complete logic circuit and automatically removes unused gates and flipflops from a logic block used in a design. This MacroMuncher feature allows you to freely employ logic blocks in your design without having to worry about optimizing their use. All inputs to TTL MacroFunctions are defined with default input signal levels so that unused inputs can simply be left unconnected.

In addition to the standard functions, this library also contains a number of EPLD-specific TTL MacroFunctions that are particularly efficient in optimizing logic functions for EPLD implementation.

The logic of some TTL MacroFunctions differs slightly from the logic of the TTL equivalents. Be sure to always check the function tables provided with each TTL MacroFunction description to see whether a particular logic block meets your requirements.

TTL MacroFunction Description

Each logic block description consists of the name assigned to the logic block (an Altera-specific name or the standard TTL number); a symbol representation; a description including syntax, available EPLDs, and default signal levels; a function table; and a logic schematic showing the logic contained in the logic block.

Figure 1-1 shows a standard symbol representation:

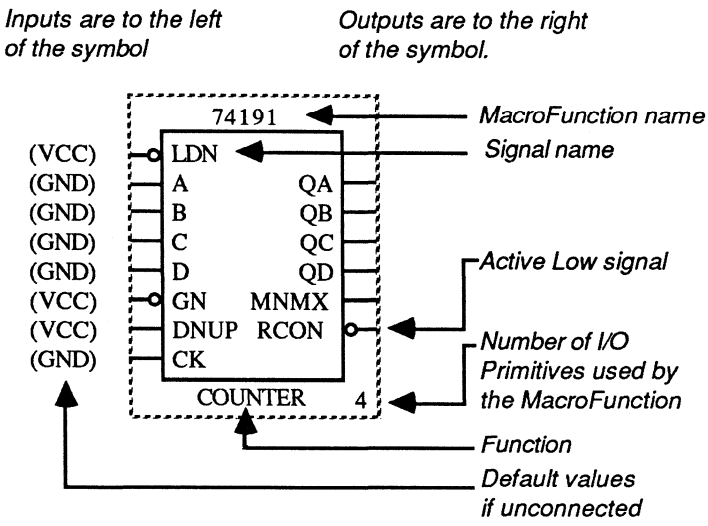


Figure 1-1. TTL MacroFunction Symbol Representation

(1) All TTL MacroFunction clocks are positive-edge triggered.

(2) All Preset inputs are synchronous presets.

The symbol representation is followed by a detailed description as outlined here:

Declaration:	Specifies the syntax for the TTL MacroFunction.
EPLDs:	Specifies for which Altera EPLDs the TTL MacroFunction may be used.
Default Signal Levels:	Indicates the default signal level for each input pin if no connection has been made. If no default is specified, it is DON'T CARE.

Next, the function table shows a table detailing the relation between the individual inputs and outputs.

Finally, the logic schematic shows a schematic of the logic within the TTL MacroFunction.

Categories of TTL MacroFunctions

If you need assistance in choosing a particular TTL MacroFunction for a specific application, please consult Table 1-1, which lists the available TTL MacroFunctions according to their functions.

Table 1-1. TTL MacroFunction Categories

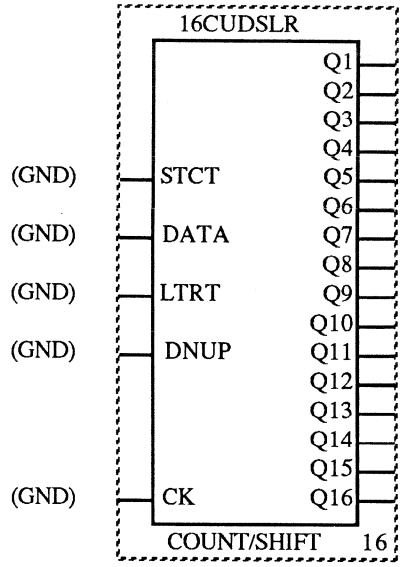
FUNCTION	AVAILABLE TTL MACROFUNCTION(S)
AND-OR Gate	7452
ALU	74181
BUS MacroFunction	COLI8, CORI8, RBUSI_A, RINP8_A
Comparator	8MCOMP, 7485, 74518
Converter	74184, 74185
Counter	16CUDSLR,4COUNT, 8COUNT, FREQDIV, GRAY4, UNICNT2, 7493, 74160, 74160T, 74161, 74161T, 74162, 74162T, 74163, 74163T, 74190, 74190T, 74191, 74191T, 74192T, 74193T, 74393
Decoder	7442, 7443, 7444, 7445, 7446, 7447, 7448, 7449, 74138, 74139, 74154, 74155, 74156
Full Adder	8FADD, 7480, 7482, 7483, 74183
I/O MacroFunction	CO2F, INPN, JO2F, RO2F, SO2F, TO2F
Latch	NANDLTCH, NORLTCH, 7475, 74116, 74259, 74279, 74373
Multiplexer	21MUX, 74147, 74148, 74151, 74153, 74157, 74158, 74298
Multiplier	MULT2, MULT24, MULT4, 74261
Parity Generator	74180, 74280
Register	7470, 7471, 7472, 7473, 7474, 7476, 7477, 7478, 74173, 74174, 74175, 74178, 74273, 74374
SSI Function	CBUF, INHB, 7400, 7402, 7404, 7408, 7410, 7411, 7420, 7421, 7427, 7430, 7432, 7486
Shift Register	BARRELST, 7491, 7494, 7496, 7499, 74164, 74165, 74166, 74179, 74194, 74198
Storage Register	7498, 74278
True Complement/ 0/1 Element	7487

SECTION 2

Reference Section

Altera TTL MacroFunctions are listed in numerical/alphabetical sequence, with Altera-specific TTL MacroFunctions listed first. All other designations correspond to those of the 74 Series of TTL circuits.

16CUDSLR (Counter)



Name: **16CUDSLR** (16-Bit Binary Up/Down Counter With Left/Right Shift Register)

Declaration: 16CUDSLR(STCT,DNUP,LTRT,DATA,CK, Q16,Q15,Q14,Q13,Q12,Q11,Q10,Q9,Q8, Q7,Q6,Q5,Q4,Q3,Q2,Q1)

(STCT = Shift/Count; DNUP = Up/Down; LTRT = Left/Right; DATA = Serial Data Input; CK = Clock)

EPLDs: EP600, EP610, EP900, EP910, EP1800, EPB1400

Default Signal Levels: GND — all input pins

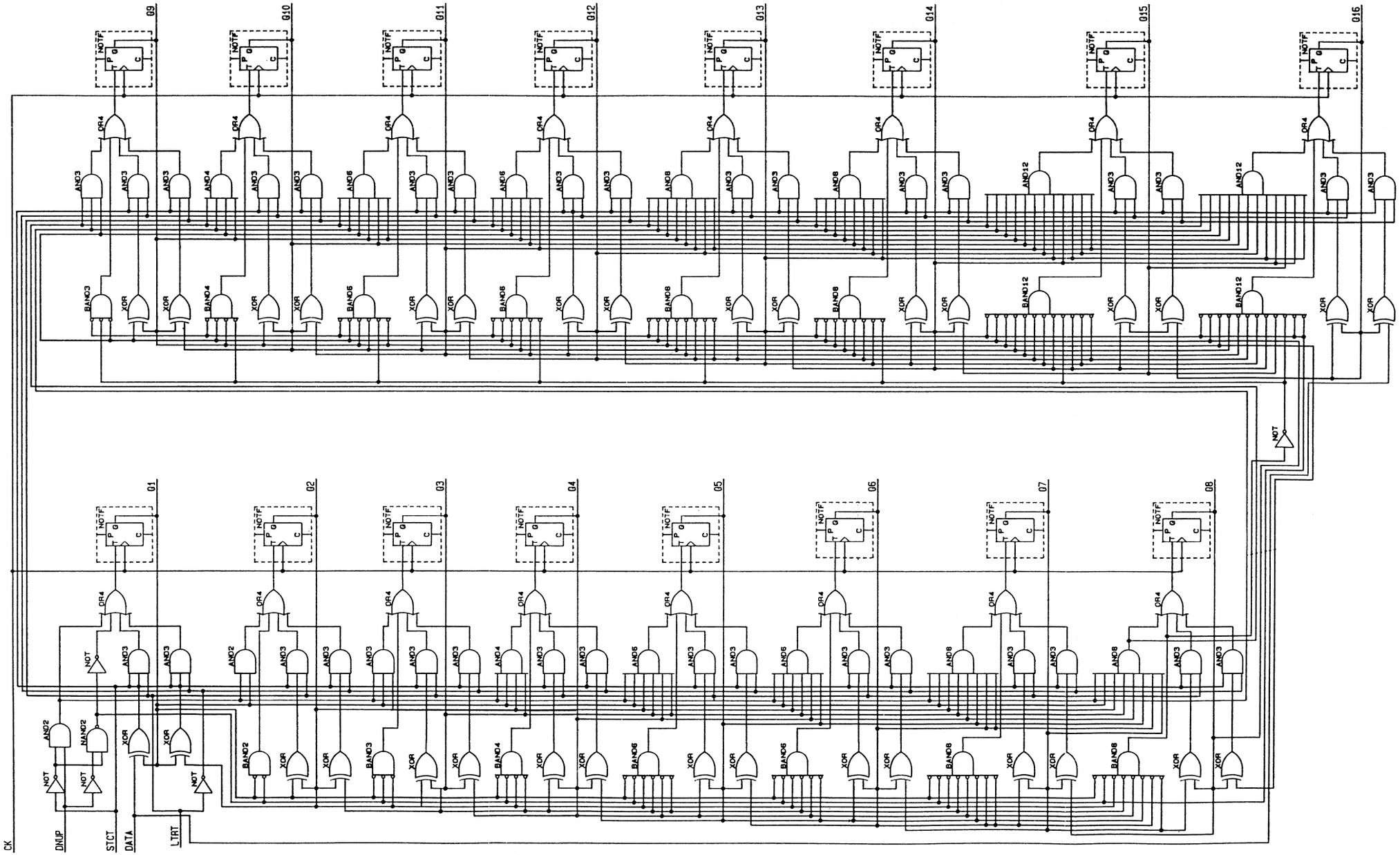
16CUDSLR Function Table:

16CUDSLR Function Table

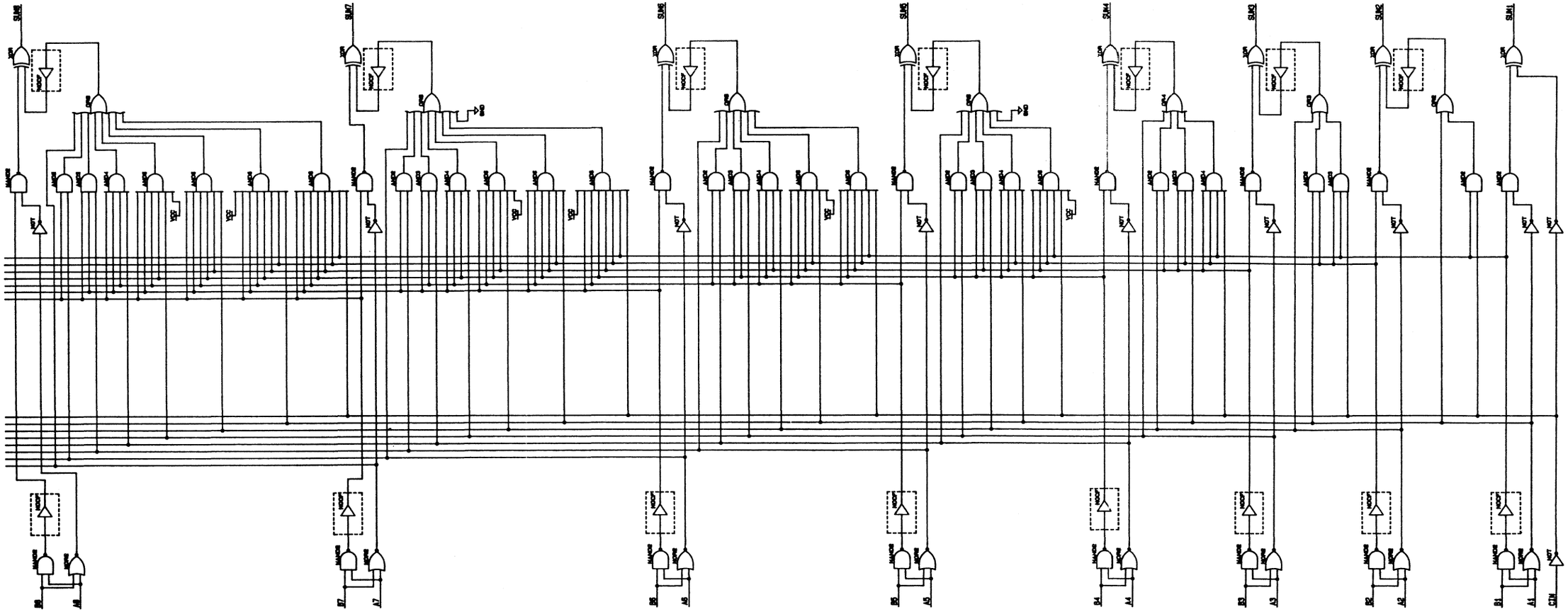
INPUTS			OPERATION
STCT	DNUP	LTRT	
H	X	H	SHIFT LEFT
H	X	L	SHIFT RIGHT
L	H	X	COUNT UP
L	L	X	COUNT DOWN

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)

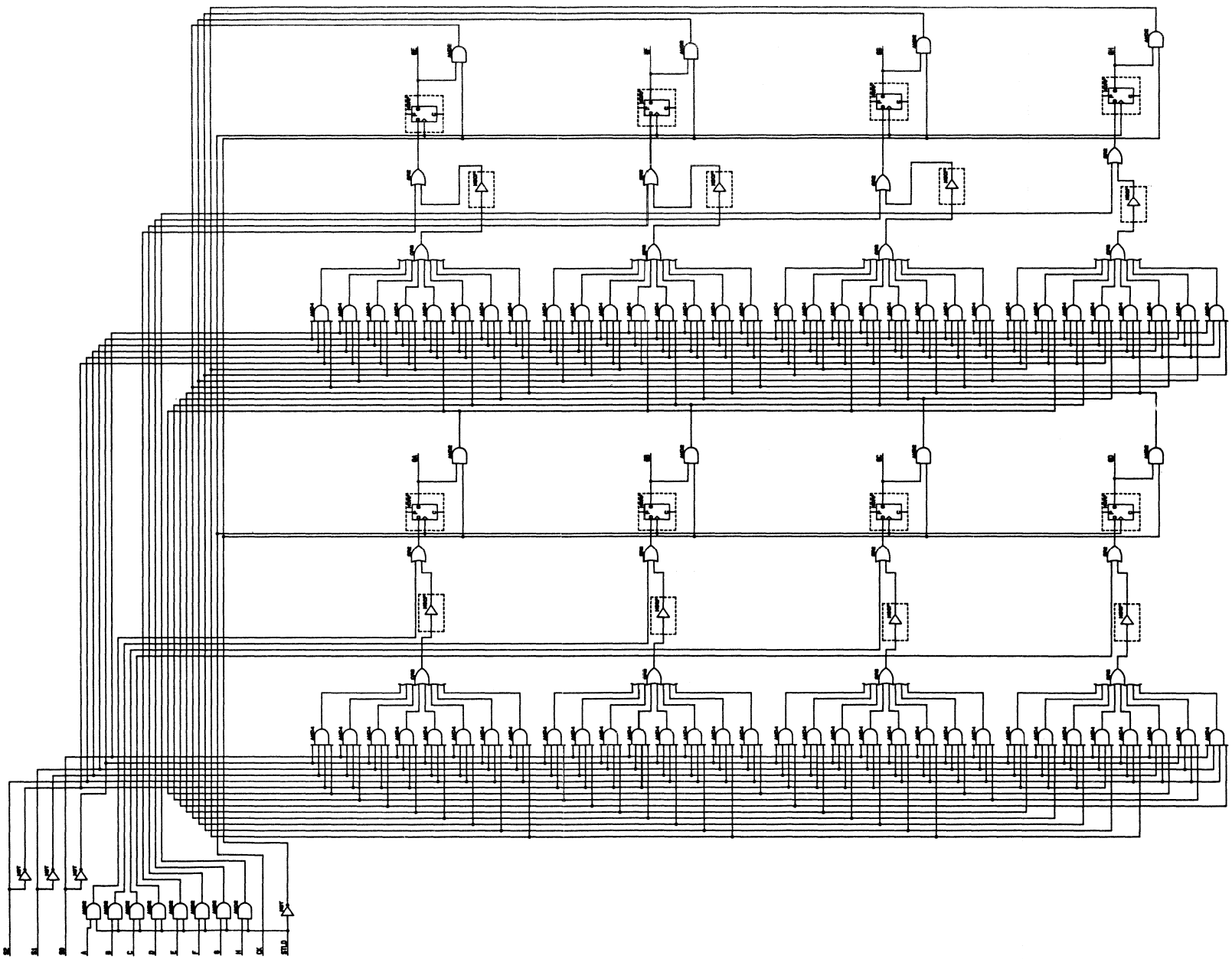
16CUDSLR Logic Schematic:



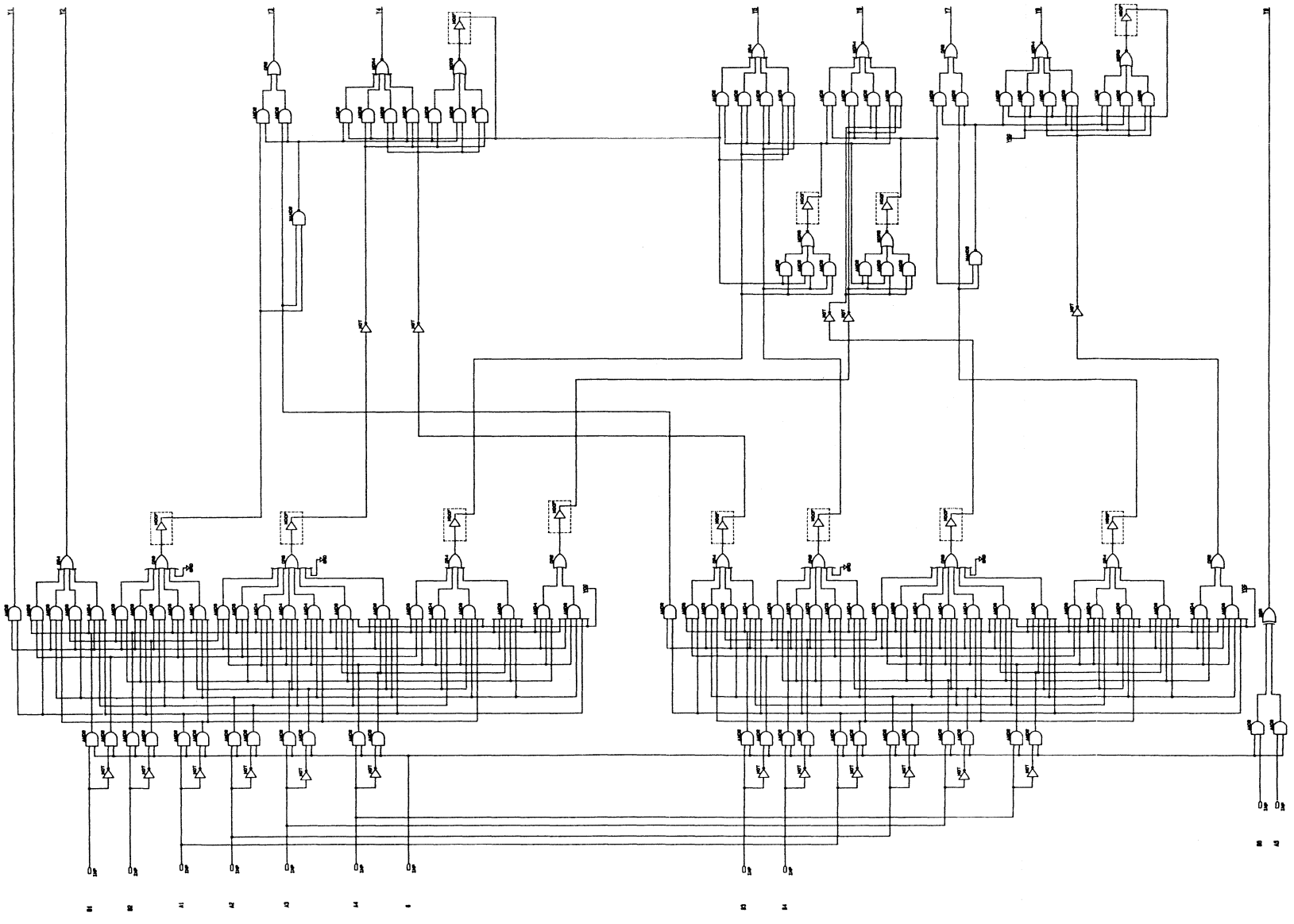
8FADD Logic Schematic:



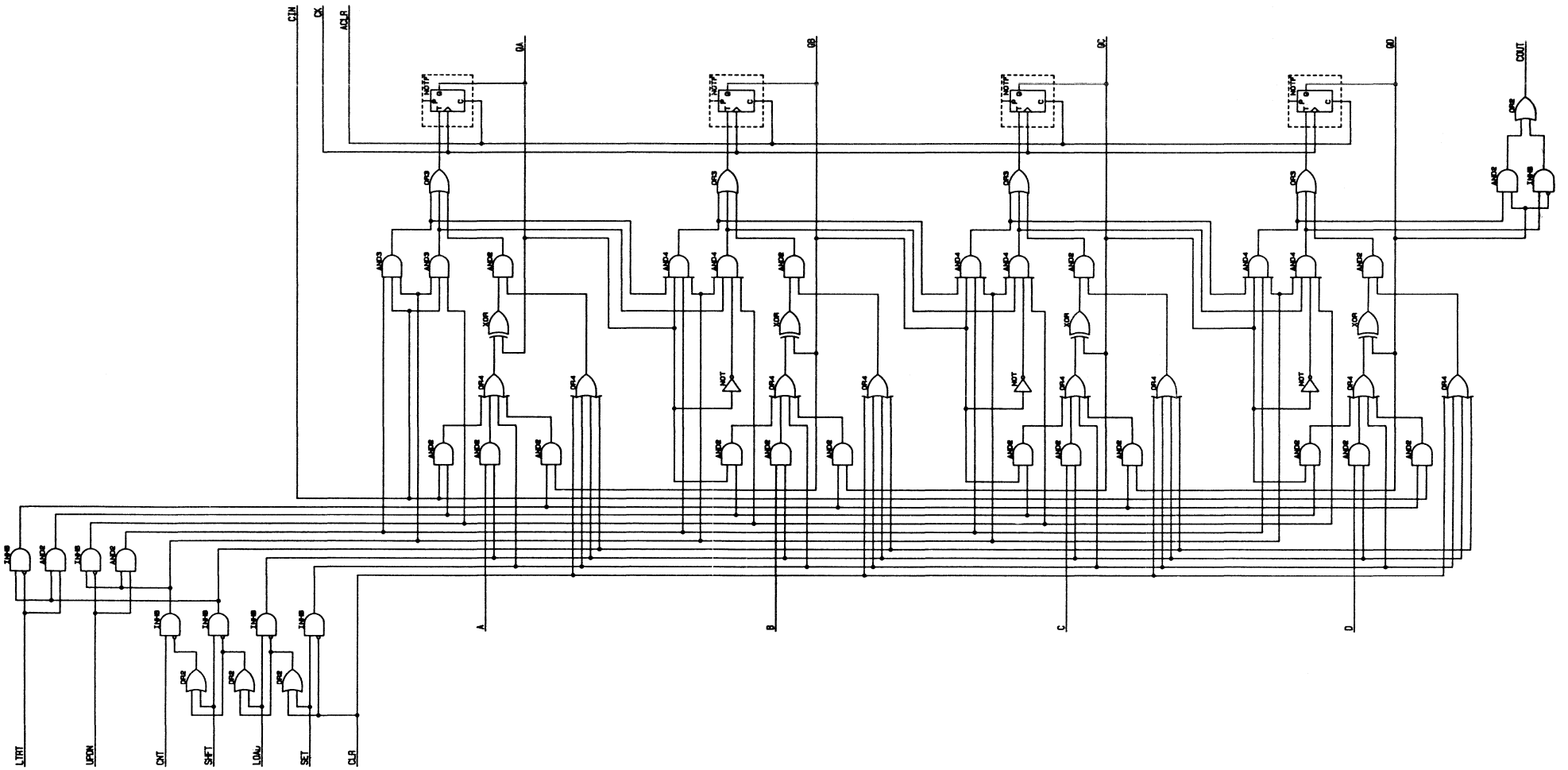
BARRELST Logic Schematic:



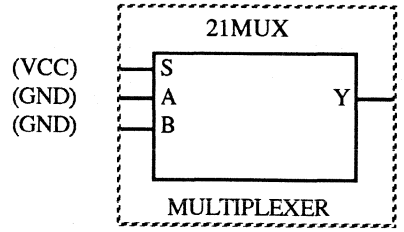
MULT4 Logic Schematic:



UNICNT2 Logic Schematic:



21MUX (Multiplexer)



Name: **21MUX** (2 to 1 Multiplexer)

Declaration: 21MUX(S,A,B,Y)

(Where: S = Select)

EPLDs: All

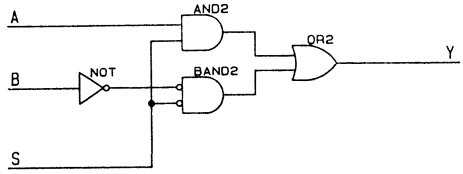
Default Signal Levels: GND — A, B
VCC — S

Function Table:

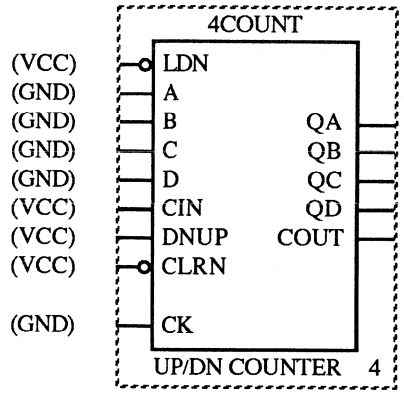
21MUX Function Table

INPUTS			OUTPUT	H = high level (steady state) L = low level (steady state) X = don't care
S	A	B	Y	
L	X	H	H	
L	X	L	L	
H	H	X	H	
H	L	X	L	

21MUX Logic Schematic:



4COUNT (Counter)



Name: **4COUNT** (4-Bit Up/Down Binary Counter With Synchronous Load and Asynchronous Clear)

Declaration: 4COUNT(CLRN,LDN,DNUP,CIN,A,B,C,D, CK,QD,QC,QB,QA,COUT)

(LDN = Load, Active Low; CIN = Carry In; DNUP = Down/Up; CLRN = Clear, Active Low; CK = Clock; COUT = Carry Out)

EPLDs: EP600, EP610, EP900, EP910, EP1800, EPB1400

Default Signal Levels: GND — CK, A, B, C, D
VCC — CLRN, LDN, DNUP,CIN

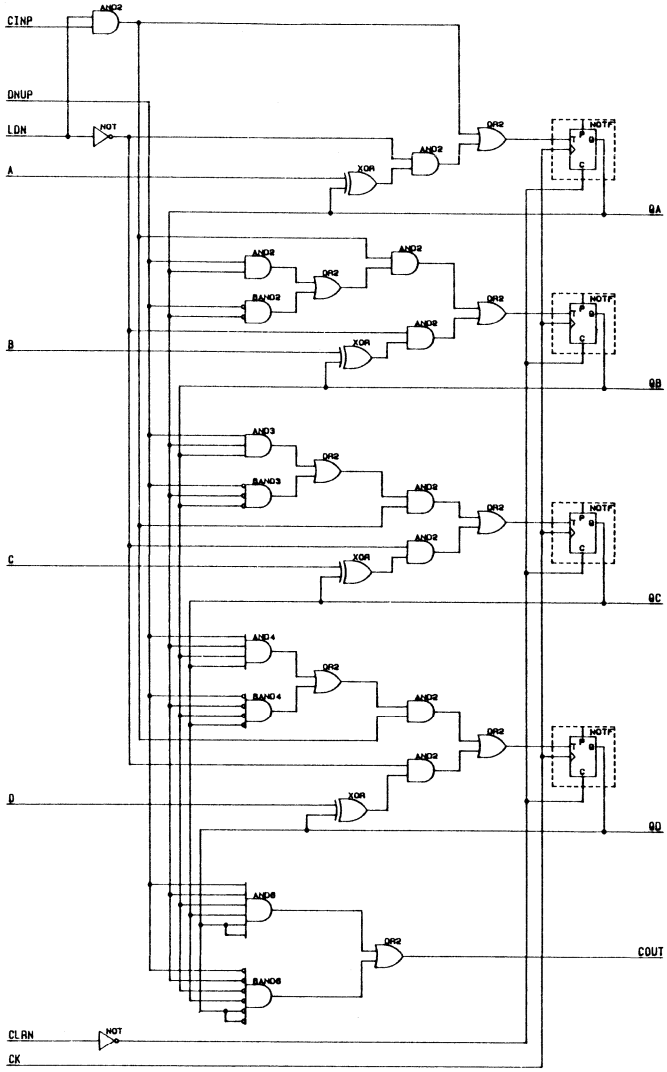
4COUNT Function Table:

4COUNT Function Table

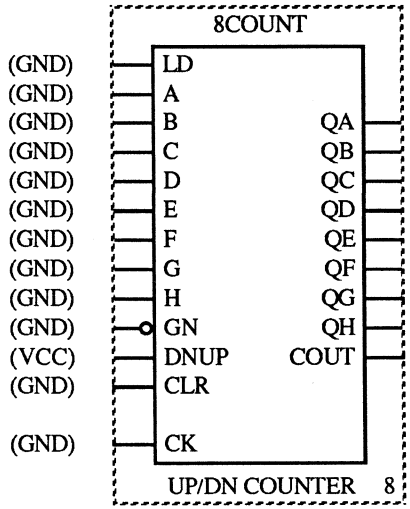
INPUTS									OUTPUTS				
CK	LDN	CLRN	DNUP	CIN	D	C	B	A	Q_D	Q_C	Q_B	Q_A	COUT
X	X	L	X	X					L	L	L	L	X
⌐	L	H	X	X	d	c	b	a	d	c	b	a	X
⌐	H	H	X	L					HOLD				X
⌐	H	H	L	H					COUNT DOWN				L
⌐	H	H	H	H					COUNT UP				L
⌐	H	H	L	H					H	H	H	H	H
⌐	H	H	H	H					L	L	L	L	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

4COUNT Logic Schematic:



8COUNT (Counter)



Name: **8 COUNT** (8-Bit Up/Down Binary Counter With Synchronous Load and Asynchronous Clear)

Declaration: 8COUNT(LD,A,B,C,D,E,F,G,H,GN,DNUP, CLR,CK,COUT,QH,QG,QF,QE,QD,QC,QB, QA)

(Where: LD = Load; GN = Enable, Active Low; DNUP = Down/Up; CLR = Clear; CK = Clock; COUT = Carry Out)

EPLDs: EP600, EP610, EP900, EP910, EP1800, EPB1400

Default Signal Levels: GND — LD, A, B, C, D, E, F, G, H, GN, CLR, CK
VCC — DNUP

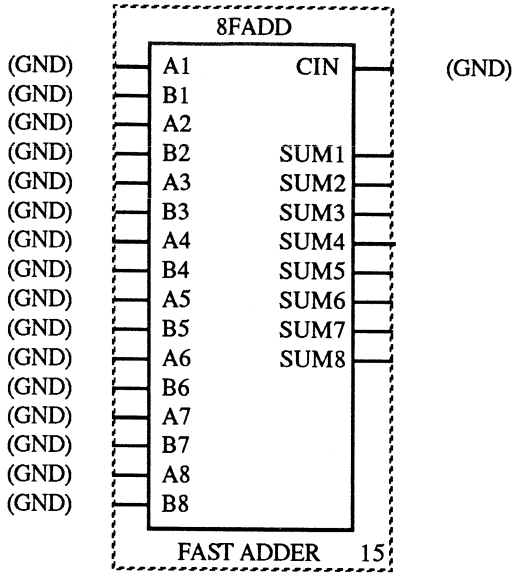
8COUNT Function Table:

8COUNT Function Table

INPUTS						OUTPUTS				
CLR	CK	GN	DNUP	LD	H G ... B A	Q_H	Q_G	... Q_B	Q_A	COUT
H	X	X	H	X		L	L	L	L	L
H	X	X	L	X		L	L	L	L	H
L	⌐	X	X	H	h g ... b a	h	g	b	a	L
L	⌐	L	H	L		COUNT UP				L
L	⌐	L	L	L		COUNT DOWN				L
L	⌐	H	X	L		HOLD COUNT				L
L	⌐	L	H	L		H	H	H	H	H
L	⌐	L	L	L		L	L	L	L	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
h, g, ... b, a = level of steady-state input at inputs H, G, ... B, A

8FADD (Adder)



Name: **8FADD** (8-Bit Full Adder)

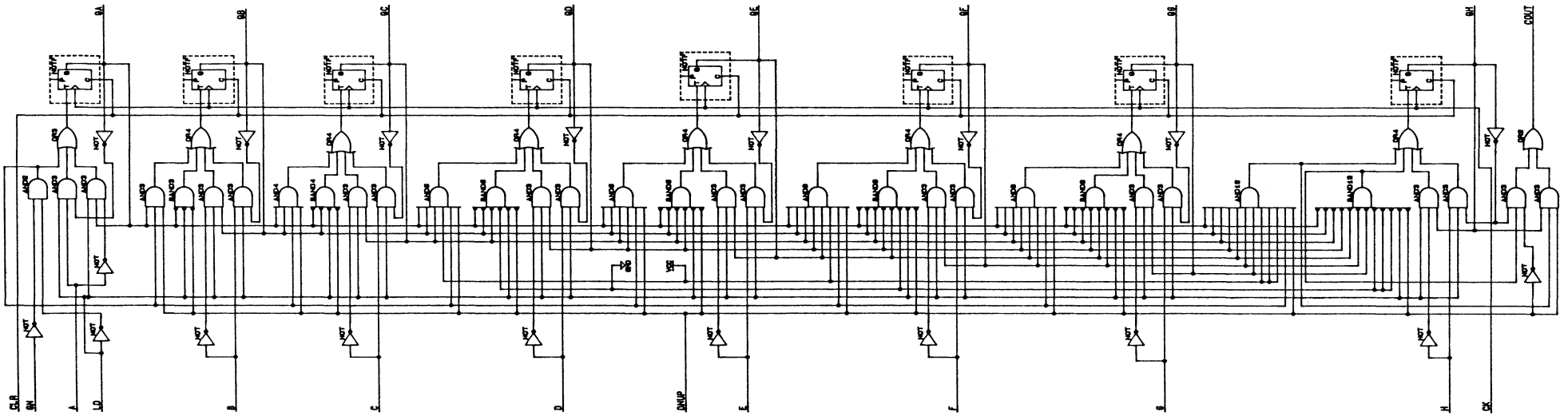
Declaration: 8FADD(A1,B1,A2,B2,A3,B3,A4,B4,A5,B5, A6,B6,A7,B7,A8,B8,SUM8,SUM7,SUM6, SUM5,SUM4,SUM3,SUM2,SUM1,CIN)

(Where: CIN = Carry In)

EPLDs: EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

8COUNT Logic Schematic:

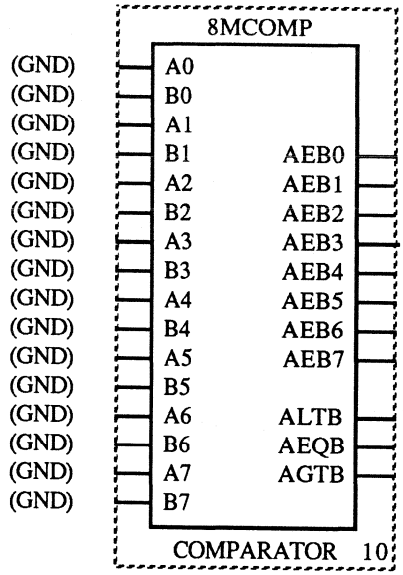


8FADD Function Table:

8FADD Function Table

INPUTS			OUTPUTS
CIN	A8 - A1	B8 - B1	SUM8 - SUM1
0	00000000	00000000	00000000
1	00000000	00000000	00000001 (CIN + A + B = SUM)
	.	.	.
	.	.	.
	.	.	.
1	00001001	00011000	00100010 (1 + 9 + 24 = 34)
	.	.	.
	.	.	.
	.	.	.

8MCOMP (Comparator)



Name: **8MCOMP** (8-Bit Magnitude Comparator)

Declaration: 8MCOMP(A0,B0,A1,B1,A2,B2,A3,B3,A4,B4, A5,B5,A6,B6,A7,B7,AGTB,AEQB,ALTB, AEB7,AEB6,AEB5,AEB4,AEB3,AEB2, AEB1,AEB0)

(AGTB = A Greater Than B; AEQB = Word A Equals Word B; ALTB = A Less Than B; AEB = Bit A Equals Bit B)

EPLDs: EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

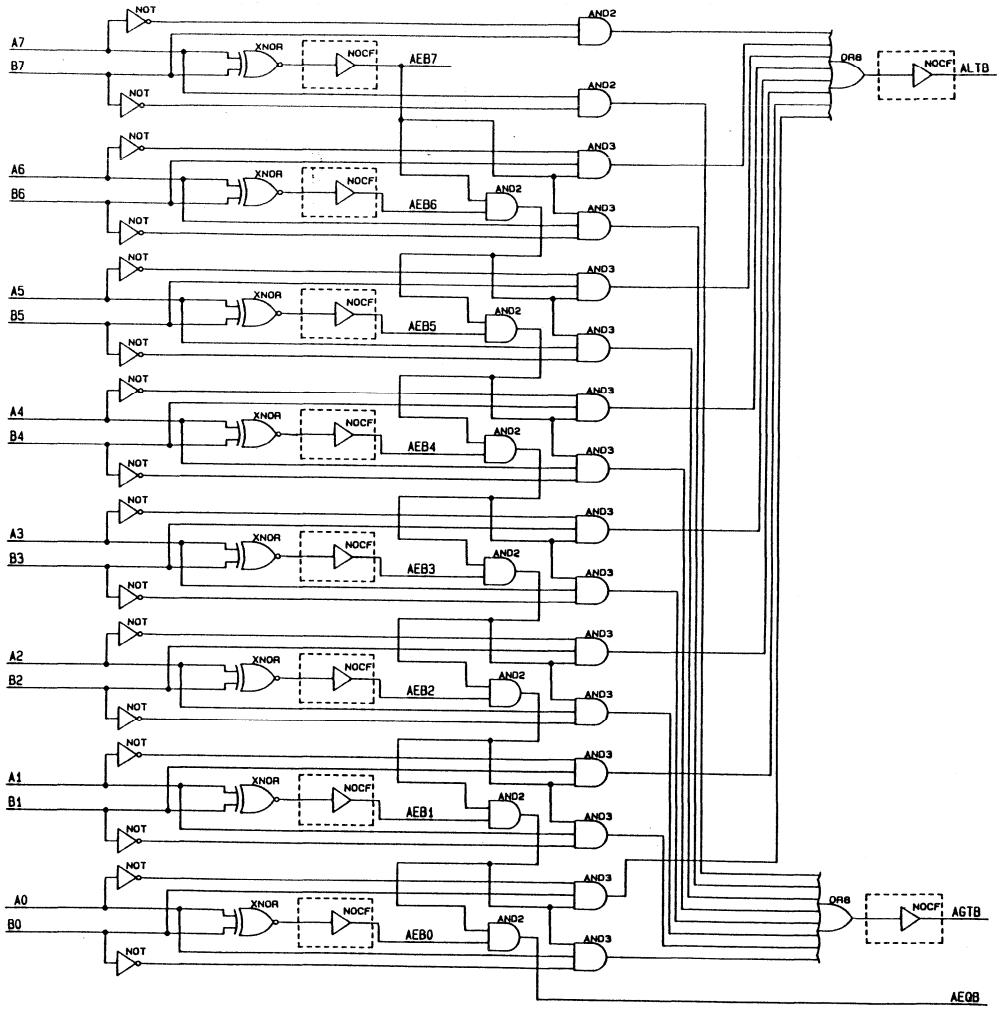
Default Signal Levels: GND — all input pins

8MCOMP Function Table:

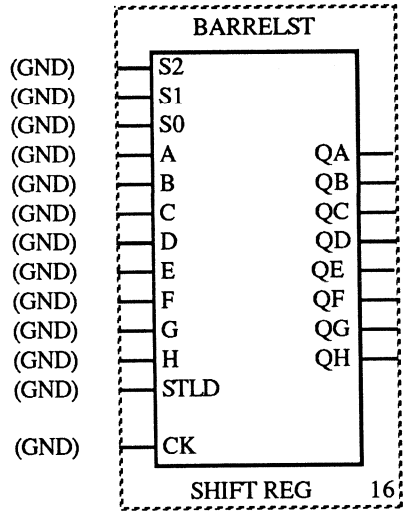
8MCOMP Function Table

INPUTS	OUTPUTS			
A B	ALTB	AEQB	AGTB	AEBx
A=B	0	1	0	
A<B	1	0	0	
A>B	0	0	1	
Ax=Bx				1
Ax≠Bx				0
x = Bit position				

8MCOMP Logic Schematic:



BARRELST (Shift Register)



Name: **BARRELST** (8-Bit Barrel Shifter)

Declaration: BARRELST(S2,S1,S0,A,B,C,D,E,F,G,H, STLD, CK,QH,QG,QF,QE,QD,QC,QB,QA)

(Where: STLD = Shift Load)

EPLDs: EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

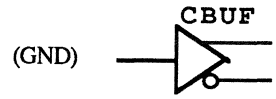
BARRELST Function Table:

BARRELST Function Table

INPUTS						OUTPUTS			
S2	S1	S0	SHIFT/ LOAD	A ... H	CLOCK	Q_A	Q_B ...	Q_G	Q_H
X	X	X	X	X	L	Q_{A0}	Q_{B0}	Q_{G0}	Q_{H0}
X	X	X	H	a ...h	⌐	a	b	g	h
L	L	L	L	X	⌐	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Hn}
L	L	H	L	X	⌐	Q_{Bn}	Q_{Cn}	Q_{Hn}	Q_{An}
L	H	L	L	X	⌐	Q_{Cn}	Q_{Dn}	Q_{An}	Q_{Bn}
L	H	H	L	X	⌐	Q_{Dn}	Q_{En}	Q_{Bn}	Q_{Cn}
H	L	L	L	X	⌐	Q_{En}	Q_{Fn}	Q_{Cn}	Q_{Dn}
H	L	H	L	X	⌐	Q_{Fn}	Q_{Gn}	Q_{Dn}	Q_{En}
H	H	L	L	X	⌐	Q_{Gn}	Q_{Hn}	Q_{En}	Q_{Fn}
H	H	H	L	X	⌐	Q_{Hn}	Q_{An}	Q_{Fn}	Q_{Gn}

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D
Q_{A0} to Q_{H0} = level of Q_A to Q_D before the indicated steady-state input conditions were established
Q_{An} to Q_{Hn} = level of Q_A to Q_H before the most recent ⌐ transition of the clock

CBUF (SSI Function)



Name: **CBUF** (Complementary Buffer)

Declaration: CBUF(Input1, Output2, Output1)

EPLDs: All

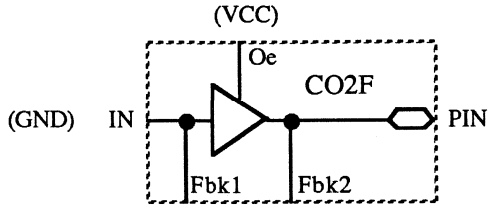
Default Signal Levels: GND — Input 1

Function Table:

CBUF Function Table

INPUT	OUTPUTS	
DATA	OUT	$\overline{\text{OUT}}$
0	0	1
1	1	0

CO2F (I/O MacroFunction)



Name: **CO2F** (Combinatorial Output, Dual Feedback)

Declaration: CO2F(PIN, IN, OE, FBK1, FBK2)

EPLDs: EP1800, EPB1400

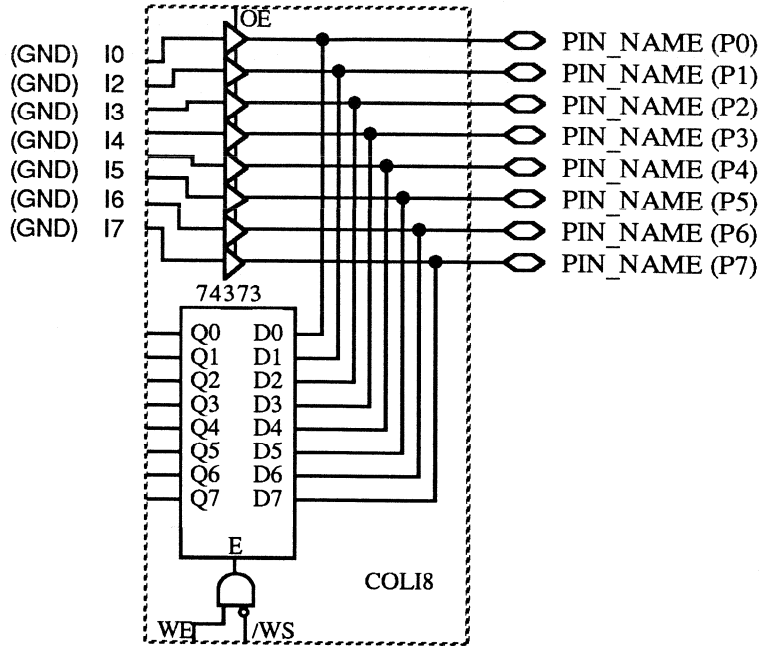
Default Signal Levels: GND — IN
VCC — OE

Function Table:

CO2F Function Table

INPUTS		OUTPUTS		
IN	OE	FBK1	PIN	FBK2
0	0	0	Z	pin
0	1	0	0	0
1	0	1	Z	pin
1	1	1	1	1
Z = high impedance				

COLI8 (BUSTER MacroFunction)



Name: **COLI8** (8-Bit Bi-Directional Port With Latched Pin Feedback and Combinatorial Output)

Declaration: COLI8(P0,P1,P2,P3,P4,P5,P6,P7,I0,I1,I2, I3,I4,I5,I6,I7,OE,Q0,Q2,Q3,Q4,Q5,Q6,Q7, WE, WS)

EPLDs: EPB1400

Default Signal Levels: GND — I0, I1, I2, I3, I4, I5, I6, I7

COLI8 Function Table:

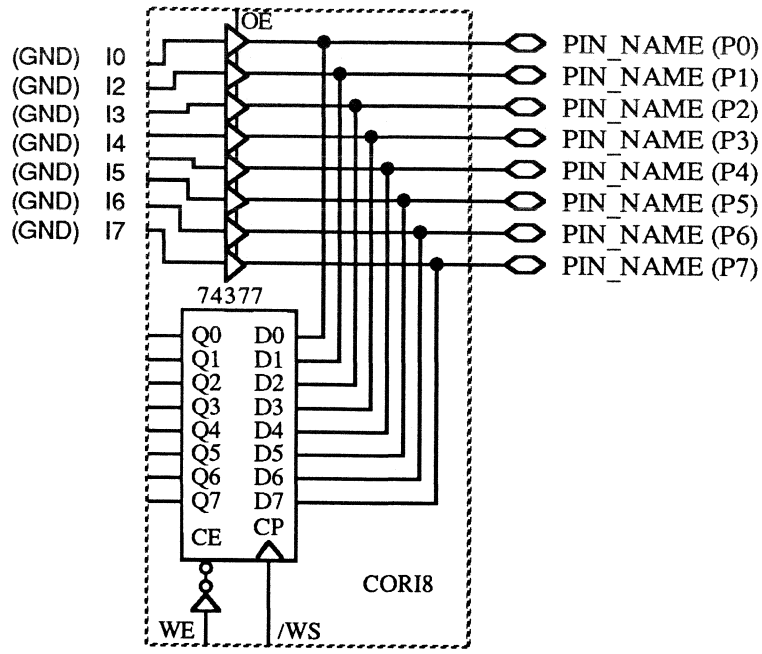
COLI8 Function Table *

OE	P0 - P7	D0 - D7
L	INPUTS	P0 - P7
H	OUTPUTS	I0 - I7

H = high level (steady state)
L = low level (steady state)

* For latch operation, see LINP8.

CORI8 (BUSTER MacroFunction)



Name: **CORI8** (8-Bit Bi-Directional Port With Registered Pin Feedback and Combinatorial Output)

Declaration: CORI8(P0,P1,P2,P3,P4,P5,P6,P7,I0,I1,I2, I3,I4,I5,I6,I7,OE,Q0,Q2,Q3,Q4,Q5,Q6,Q7, WS, WE)

EPLDs: EPB1400

Default Signal Levels: GND — I0, I1, I2, I3, I4, I5, I6, I7

CORI8 Function Table:

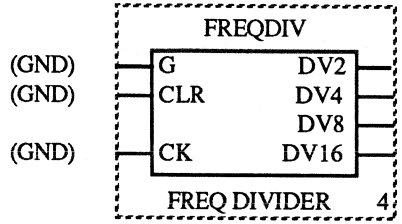
CORI8 Function Table*

OE	P0 - P7	D0 - D7
L	INPUTS	P0 - P7
H	OUTPUTS	I0 - I7

H = high level (steady state)
L = low level (steady state)

* For register operation, see RINP8.

FREQDIV (Frequency Divider)



Name: **FREQDIV** (Frequency Divider)

Declaration: FREQDIV(G,CLR,CK,DV16,DV8,DV4,DV2)

(Where: CLR = Clear)

EPLDs: EP600, EP610, EP900, EP910, EP1800, EPB1400

Default Signal Levels: GND — all input pins

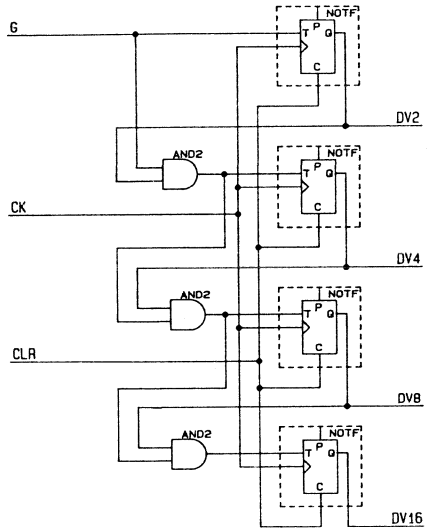
Function Table:

FREQDIV Function Table

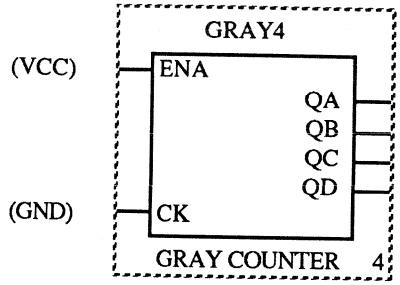
INPUTS			OUTPUTS			
CLR	CK	G	DV2	DV4	DV8	DV16
H	X	X	L	L	L	L
L	⌐	L	$DV2_0$	$DV4_0$	$DV8_0$	$DV16_0$
L	⌐	H	H_2	H_4	H_8	H_{16}

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
H_2 = high every other clock pulse
H_4 = high every 4 clock pulses
H_8 = high every 8 clock pulses
H_{16} = high every 16 clock pulses

FREQDIV Logic Schematic:



GRAY4 (Counter)



Name:	**GRAY4** (Graycode Counter)
Declaration:	GRAY4(CK,ENA,QD,QC,QB,QA)
	(Where: ENA = Enable)
EPLDs:	EP600, EP610, EP900, EP910, EP1800
Default Signal Levels:	GND — CK VCC — ENA

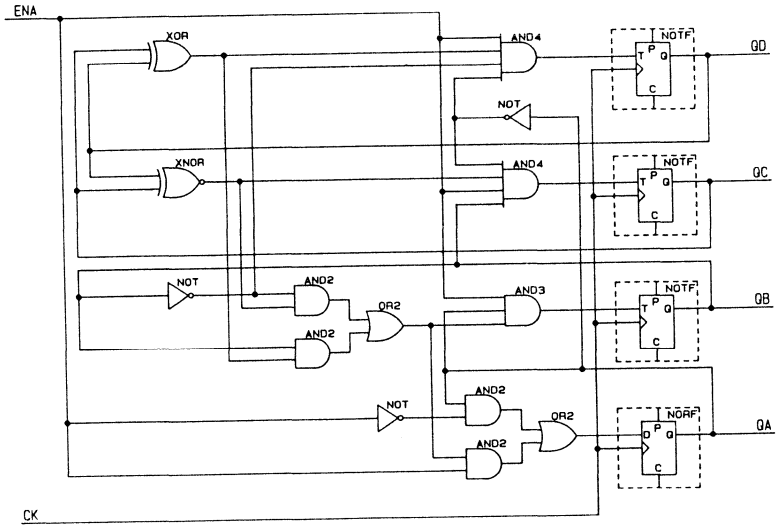
GRAY4 Function Table:

GRAY4 Function Table

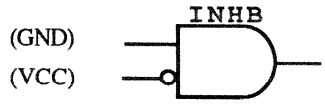
INPUTS		OUTPUTS			
CK	ENA	Q_D	Q_C	Q_B	Q_A
X	0	HOLD COUNT			
⌐	1	0	0	0	0
⌐	1	0	0	0	1
⌐	1	0	0	1	1
⌐	1	0	0	1	0
⌐	1	0	1	1	0
⌐	1	0	1	1	1
⌐	1	0	1	0	1
⌐	1	1	0	0	0
⌐	1	1	1	0	0
⌐	1	1	1	0	1
⌐	1	1	1	1	1
⌐	1	1	1	1	0
⌐	1	1	0	1	0
⌐	1	1	0	1	1
⌐	1	1	0	0	1
⌐	1	1	0	0	0

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level

GRAY4 Logic Schematic:



INHB (SSI Function)



Name: **INHB** (Inhibit)

Declaration: INHB(IN1,IN2,OUT)

EPLDs: All

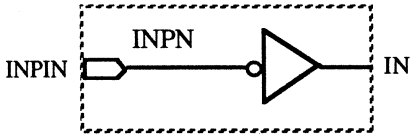
Default Signal Levels: GND — Input 1
VCC — Input 2

Function Table:

INHB Function Table

INPUTS		OUTPUT
IN1	$\overline{IN2}$	
0	0	0
0	1	0
1	0	1
1	1	0

INPN (I/O MacroFunction)



Name: **INPN** (Active Low Input)

Declaration: INPN(INPIN,IN)

EPLDs: All

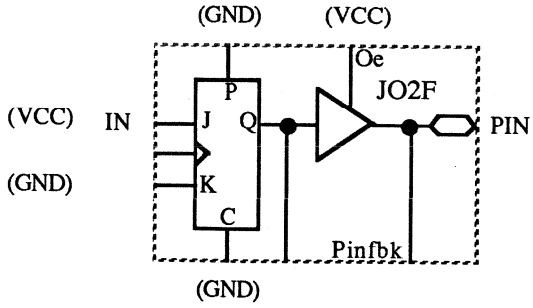
Default Signal Levels: none

Function Table:

INPN Function Table

INPIN	IN
0	1
1	0

JO2F (I/O MacroFunction)



Name: **JO2F** (JK Output, Dual Feedback)

Declaration: JO2F(PIN,J,CLK,K,C,P,OE,Q,PINFBK)

EPLDs: EP1800, EPB1400

Default Signal Levels: GND — K, C, P
VCC — J, OE

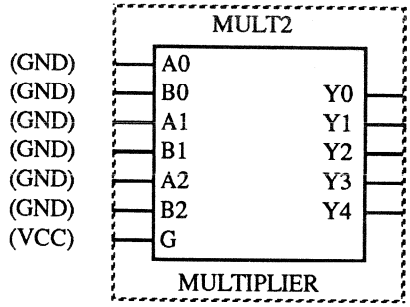
JO2F Function Table:

JO2F Function Table

INPUTS						OUTPUTS	
CLOCK	CLEAR	PRESET	J	K	OE	Q FBK	PINFBK
X	H	X	X	X	H	L	L
X	H	X	X	X	L	L	Z (input)
⌐	L	X	L	L	H	Q_O	Q_O
⌐	L	X	L	L	L	Q_O	Z (input)
⌐	L	X	L	H	H	L	L
⌐	L	X	L	H	L	L	Z (input)
⌐	L	X	H	L	H	H	H
⌐	L	X	H	L	L	H	Z (input)
⌐	L	X	H	H	H	$\overline{Q_O}$	$\overline{Q_O}$
⌐	L	X	H	H	L	$\overline{Q_O}$	Z (input)

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
Z = high impedance

MULT2 (Multiplier)



Name: **MULT2** (2-Bit Sign Magnitude Multiplier)

Declaration: MULT2(A0,B0,A1,B1,A2,B2,G,Y4,Y3,Y2, Y1,Y0)

EPLDs: All

Default Signal Levels: GND — A0,B0,A1,B2,A2,B2
VCC — G

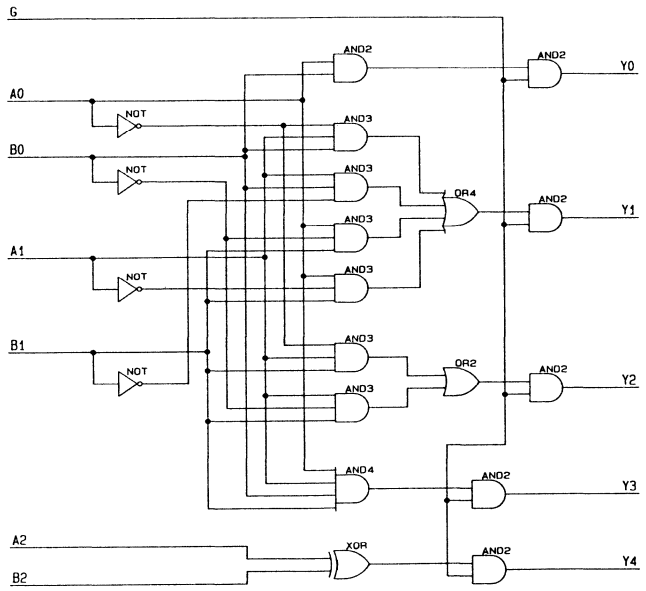
MULT2 Function Table:

MULT2 Function Table

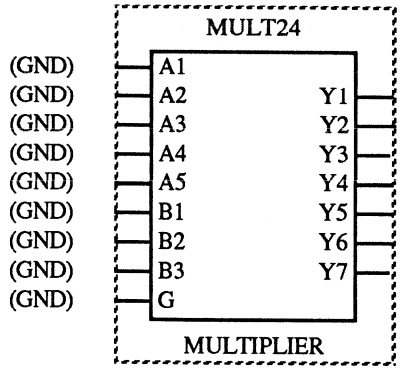
INPUTS							OUTPUTS				
A2*	A1	A0	B2*	B1	B0	G	Y4*	Y3	Y2	Y1	Y0
X	X	X	X	X	X	L	L	L	L	L	L
L	a1	a0	L	b1	b0	H	L				
L	a1	a0	H	b1	b0	H	H	A MULTIPLIED BY B			
H	a1	a0	L	b1	b0	H	H				
H	a1	a0	H	b1	b0	H	L				

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
*sign bits for sign-magnitude multiplication

MULT2 Logic Schematic:



MULT24 (Multiplier)



Name: **MULT24** (2-Bit by 4-Bit Parallel Binary Multiplier)

Declaration: MULT24(A1,A2,A3,A4,A5,B1,B2,B3,G,Y7, Y6,Y5,Y4,Y3,Y2,Y1)

EPLDs: All

Default Signal Levels: GND — all input pins

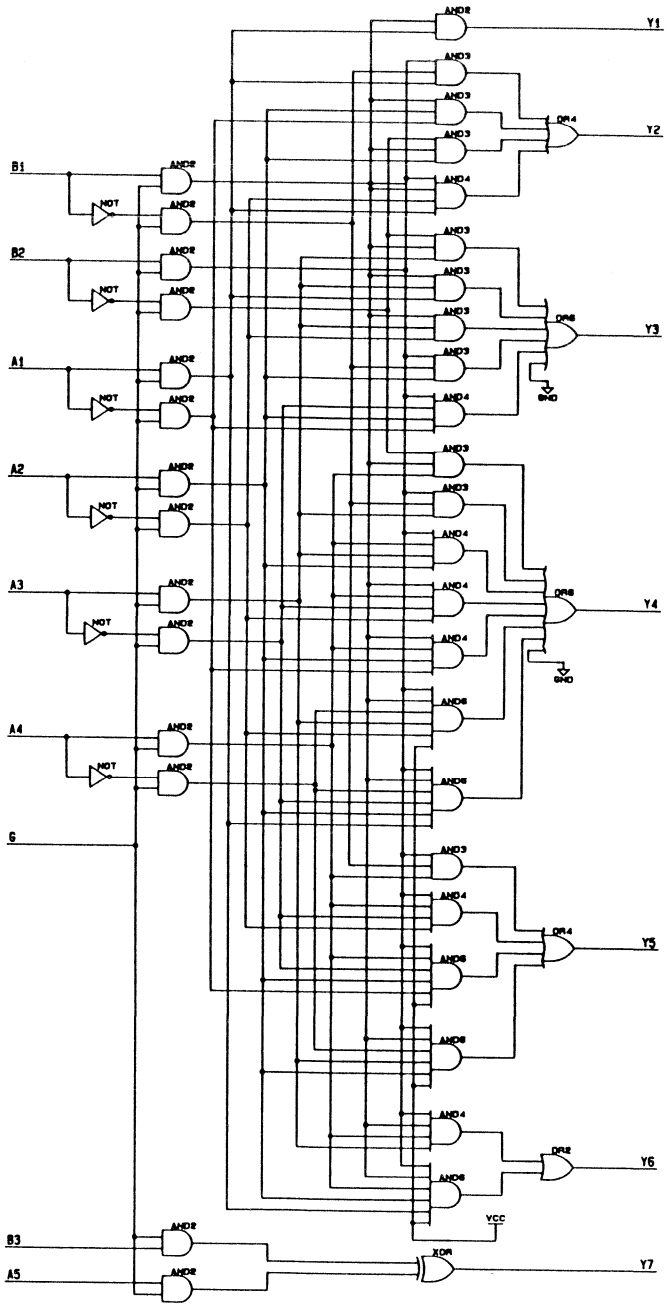
MULT24 Function Table:

MULT24 Function Table

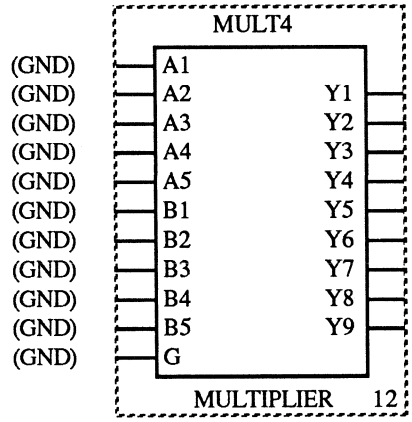
INPUTS									OUTPUTS						
A5*	A4	A3	A2	A1	B3*	B2	B1	G	Y7*	Y6	Y5	Y4	Y3	Y2	Y1
X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L
L	a4	a3	a2	a1	L	b2	b1	H	L						
L	a4	a3	a2	a1	H	b2	b1	H	H			A MULTIPLIED BY B			
H	a4	a3	a2	a1	L	b2	b1	H	H						
H	a4	a3	a2	a1	H	b2	b1	H	L						

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
*sign bits for sign-magnitude multiplication

MULT24 Logic Schematic:



MULT4 (Multiplier)



Name: **MULT4** (4-Bit Parallel Binary Multiplier)

Declaration: MULT4(A1,A2,A3,A4,A5,B1,B2,B3,B4,B5, G,Y9,Y8,Y7,Y6,Y5,Y4,Y3,Y2,Y1)

EPLDs: EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

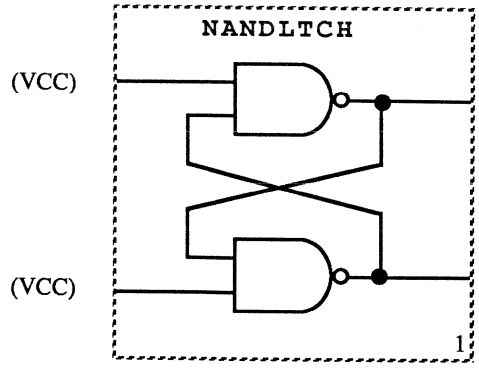
MULT4 Function Table:

MULT4 Function Table

INPUTS						OUTPUTS	
A5*	A4 ... A1		B5*	B4 ... B1		G	Y9*	Y8 ... Y1
X	X	X	X	X	X	L	L	L ... L
L	a4	a1	L	b4	b1	H	L	
L	a4	a1	H	b4	b1	H	H	A MULTIPLIED BY B
H	a4	a1	L	b4	b1	H	H	
H	a4	a1	H	b4	b1	H	L	

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
*sign bits for sign-magnitude multiplication

NANDLTCH (Latch)



Name: **NANDLTCH**

Declaration: NANDLTCH(SETn,RESETn,Q,Qn)

EPLDs: All

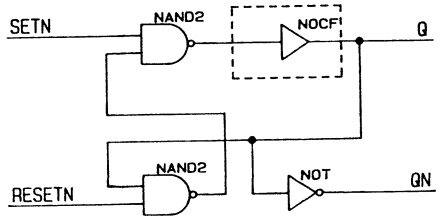
Default Signal Levels: VCC — all input pins

Function Table:

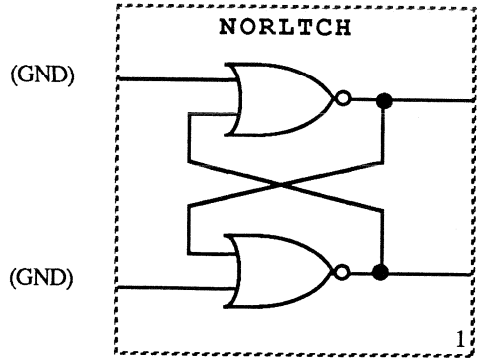
NANDLTCH Function Table

INPUTS		OUTPUTS	
/SET	/RESET	Q	/Q
0	0	1	0
0	1	1	0
1	0	0	1
1	1	Q	/Q

NANDLTCH Logic Schematic:



NORLTCH (Latch)



Name: **NORLTCH**

Declaration: NORLTCH(RESET,SET,Q,Qn)

EPLDs: All

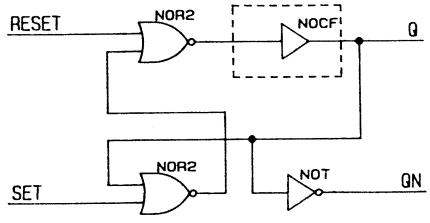
Default Signal Levels: GND — all input pins

Function Table:

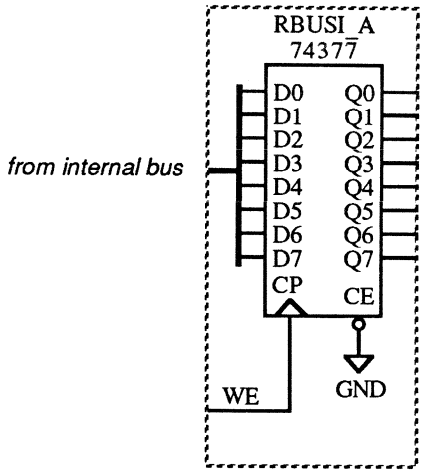
NORLTCH Function Table

INPUTS		OUTPUTS	
SET	RESET	Q	/Q
0	0	Q	/Q
0	1	0	1
1	0	1	0
1	1	0	1

NORLTCH Logic Schematic:



RBUSI_A (BUSTER MacroFunction)



Name: **RBUSI_A** (Registered Bus Input to Logic)

Declaration: RBUSI_A(INP BUS,WE,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7)

EPLDs: EPB1400

Default Signal Levels: none

☞ Write Enable and Bus *must* be connected.

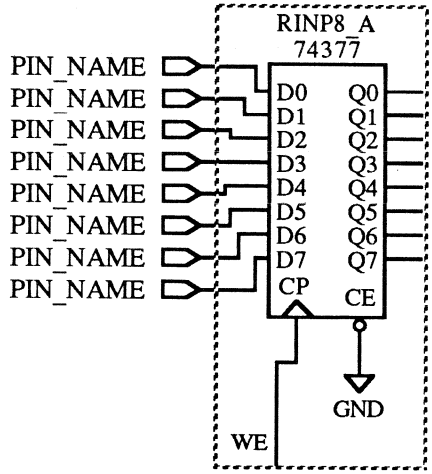
RBUSI_A Function Table:

RBUSI_A Function Table

INPUTS			OUTPUTS
WE	INP BUS	Q	Q0 - Q7
⌐	L	X	L
⌐	H	X	H
L	X	L	L
L	X	H	H
H	X	L	L
H	X	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level

RINP8_A (BUSTER MacroFunction)



Name: **RINP8_A** (8-Bit Registered Pin Input to Logic)

Declaration: RINP8_A(IN1,IN2,IN3,IN4,IN5,IN6,IN7,IN8, WE,Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7)

EPLDs: EPB1400

Default Signal Levels: none

☞ WE and Inputs *must* be connected.

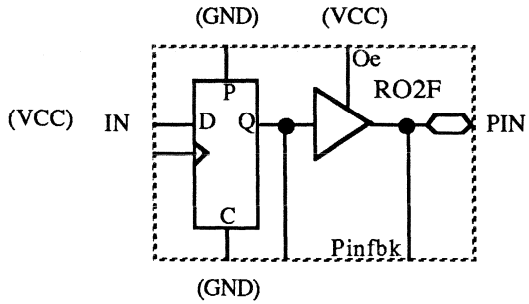
RINP8_A Function Table:

RINP8_A Function Table

INPUTS			OUTPUTS
WE	D	Q	Q0 - Q7
⌐	L	X	L
⌐	H	X	H
L	X	L	L
L	X	H	H
H	X	L	L
H	X	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level

RO2F (I/O MacroFunction)



Name: **RO2F** (Registered Output, Dual Feedback)

Declaration: RO2F(PIN,D,CLK,C,P,OE,Q,PINFBK)

EPLDs: EP1800, EPB1400

Default Signal Levels: GND — C, P
VCC — D, OE

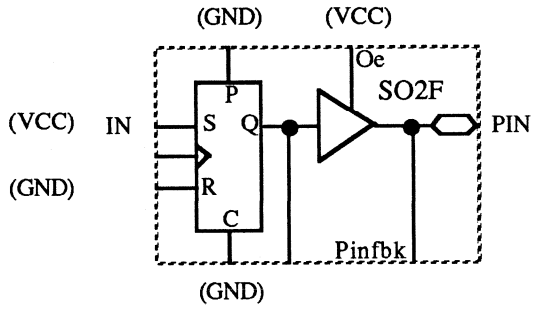
Function Table:

RO2F Function Table

INPUTS					OUTPUTS	
CLOCK	CLEAR	PRESET	D	OE	Q FBK	I/O PINFBK
X	H	X	X	H	L	L
X	H	X	X	L	L	Z (input)
⌐	L	X	H	H	H	H
⌐	L	X	H	L	H	Z (input)
⌐	L	X	L	H	L	L
⌐	L	X	L	L	L	Z (input)

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
Z = high impedance

SO2F (I/O MacroFunction)



Name: **SO2F** (SR Output, Dual Feedback)

Declaration: SO2F(PIN,S,CLK,R,C,P,OE,Q,PINFBK)

EPLDs: EP1800, EPB1400

Default Signal Levels: GND — R, C, P
VCC — S, OE

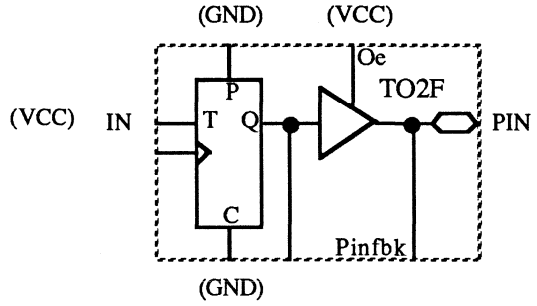
SO2F Function Table:

SO2F Function Table

INPUTS						OUTPUTS	
CLOCK	CLEAR	PRESET	S	R	OE	Q FBK	I/O PINFBK
X	H	X	X	X	H	L	L
X	H	X	X	X	L	L	Z (input)
⌐	L	X	L	L	H	Q_O	Q_O
⌐	L	X	L	L	L	Q_O	Z (input)
⌐	L	X	L	H	H	L	L
⌐	L	X	L	H	L	L	Z (input)
⌐	L	X	H	L	H	H	H
⌐	L	X	H	L	L	H	Z (input)
⌐	L	X	H	H	H	U	U
⌐	L	X	H	H	L	U	Z(input)

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
Z = high impedance
U = undefined

TO2F (I/O MacroFunction)



Name: **TO2F** (T Output, Dual Feedback)

Declaration: TO2F(PIN,T,CLK,C,P,OE,Q,PINFBK)

EPLDs: EP1800, EPB1400

Default Signal Levels: GND — C, P
VCC — T, OE

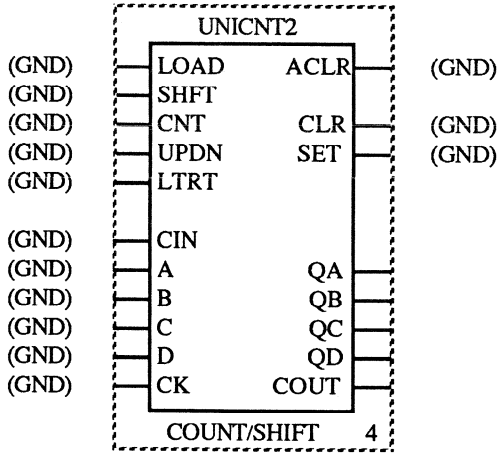
Function Table:

TO2F Function Table

INPUTS					OUTPUTS	
CLOCK	CLEAR	PRESET	T	OE	Q FBK	I/O PINFBK
X	H	X	X	H	L	L
X	H	X	X	L	L	Z (input)
⌐	L	X	H	H	$\overline{Q_O}$	$\overline{Q_O}$
⌐	L	X	H	L	$\overline{Q_O}$	Z (input)
⌐	L	X	L	H	Q_O	$\overline{Q_O}$
⌐	L	X	L	L	Q_O	Z (input)

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
Z = high impedance

UNICNT2 (Counter)



Name: **UNICNT2** (Universal 4-Bit Up/Down Counter, Left/Right Shift Register with Load, Clear; Cascade)

Declaration: UNICNT2(LOAD,SHFT,CNT,UPDN,LTRT, CIN,A,B,C,D,CK,COUT,QD,QC,QB,QA, SET, CLR,ACLR)

(Where: LOAD = Load; SHFT = Shift; CNT = Count; UPDN = Up/Down; LTRT = Left/Right; CIN = Count In; CK = Clock; ACLR = Asynchronous Clear; CLR = Clear; SET = Set; COUT = Carry Out)

EPLDs: EP600, EP610, EP900, EP910, EP1800, EPB1400

Default Signal Levels: GND — all input pins

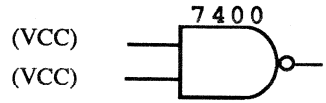
UNICNT2 Function Table:

UNICNT2 Function Table

INPUTS									OUTPUTS				
CK	ACLR	CLR	SET	LOAD	SHFT	LTRT	CNT	UPDN	Q_D	Q_C	Q_B	Q_A	COUT
X	1	X	X	X	X	X	X	X	0	0	0	0	X
⌐	0	1	X	X	X	X	X	X	0	0	0	0	/UPDN
⌐	0	0	1	X	X	X	X	X	1	1	1	1	UPDN
⌐	0	0	0	1	X	X	X	X	d	c	b	a	0
⌐	0	0	0	0	1	1	X	X	CIN	QD	QC	QB	0
⌐	0	0	0	0	1	0	X	X	QC	QB	QA	CIN	0
⌐	0	0	0	0	0	X	1	1	4-Bit Binary Up Counter				
⌐	0	0	0	0	0	X	1	0	4-Bit Binary Down Counter				

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

7400 (SSI Function)



Name: **7400** (NAND2)

Declaration: 7400(A,B,OUT)

EPLDs: All

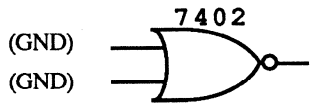
Default Signal Levels: VCC — all input pins

Function Table:

7400 Function Table

INPUTS		OUTPUT
B	A	
0	0	1
0	1	1
1	0	1
1	1	0

7402 (SSI Function)



Name: **7402** (NOR2)

Declaration: 7402(A,B,OUT)

EPLDs: All

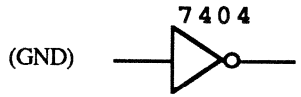
Default Signal Levels: GND — all input pins

Function Table:

7402 Function Table

INPUTS		OUTPUT
B	A	
0	0	1
0	1	0
1	0	0
1	1	0

7404 (SSI Function)



Name: **7404** (NOT)

Declaration: 7404(IN,OUT)

EPLDs: All

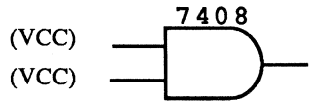
Default Signal Levels: GND — input pin

Function Table:

7404 Function Table

INPUT	OUTPUT
0	1
1	0

7408 (SSI Function)



Name: **7408** (AND2)

Declaration: 7408(A,B,OUT)

EPLDs: All

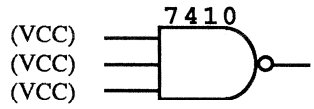
Default Signal Levels: VCC — all input pins

Function Table:

7408 Function Table

INPUTS		OUTPUT
B	A	
0	0	0
0	1	0
1	0	0
1	1	1

7410 (SSI Function)



Name: **7410** (NAND3)

Declaration: 7410(A,B,C,OUT)

EPLDs: All

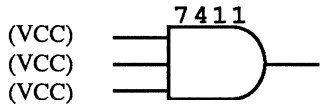
Default Signal Levels: VCC — all input pins

Function Table:

7410 Function Table

INPUTS			OUTPUT
C	B	A	
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

7411 (SSI Function)



Name: **7411** (AND3)

Declaration: 7411(A,B,C,OUT)

EPLDs: All

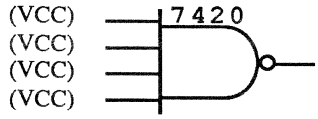
Default Signal Levels: VCC — all input pins

Function Table:

7411 Function Table

INPUTS			OUTPUT
C	B	A	
X	X	0	0
X	0	X	0
0	X	X	0
1	1	1	1

7420 (SSI Function)



Name: **7420** (NAND4)

Declaration: 7420(A,B,C,D,OUT)

EPLDs: All

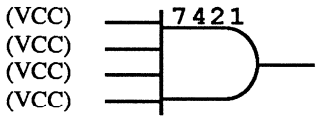
Default Signal Levels: VCC — all input pins

Function Table:

7420 Function Table

INPUTS				OUTPUT
D	C	B	A	
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	1	0

7421 (SSI Function)



Name: **7421** (AND4)

Declaration: 7421(A,B,C,D,OUT)

EPLDs: All

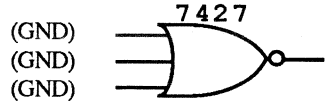
Default Signal Levels: VCC — all input pins

Function Table:

7421 Function Table

INPUTS				OUTPUT
D	C	B	A	
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	1	1

7427 (SSI Function)



Name: **7427** (NOR3)

Declaration: 7427(A,B,C,OUT)

EPLDs: All

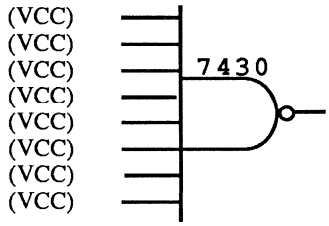
Default Signal Levels: GND — all input pins

Function Table:

7427 Function Table

INPUTS			OUTPUT
C	B	A	
X	X	1	0
X	1	X	0
1	X	X	0
0	0	0	1

7430 (SSI Function)



Name: **7430** (NAND8)

Declaration: 7430(A,B,C,D,E,F,G,H,OUT)

EPLDs: All

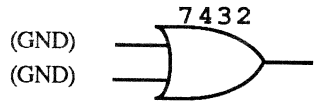
Default Signal Levels: VCC — all input pins

Function Table:

7430 Function Table

INPUTS								OUTPUT
H	G	F	E	D	C	B	A	
X	X	X	X	X	X	X	0	1
X	X	X	X	X	X	0	X	1
X	X	X	X	X	0	X	X	1
X	X	X	X	0	X	X	X	1
X	X	X	0	X	X	X	X	1
X	X	0	X	X	X	X	X	1
X	0	X	X	X	X	X	X	1
0	X	X	X	X	X	X	X	1
1	1	1	1	1	1	1	1	0

7432 (SSI Function)



Name: **7432** (OR2)

Declaration: 7432(A,B,OUT)

EPLDs: All

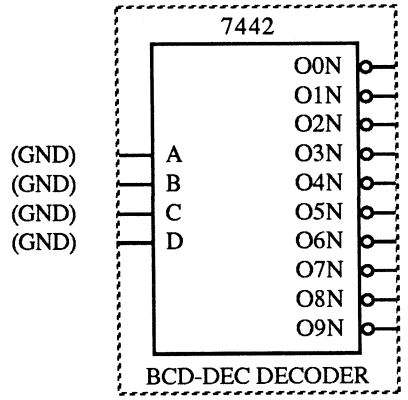
Default Signal Levels: GND — all input pins

Function Table:

7432 Function Table

INPUTS		OUTPUT
B	A	
0	0	0
0	1	1
1	0	1
1	1	1

7442 (Decoder)



Name: **7442** (1:10 BCD to Decimal Decoder)

Declaration: 7442(A,B,C,D,O9N,O8N,O7N,O6N,O5N, O4N, O3N,O2N,O1N,O0N)

EPLDs: EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

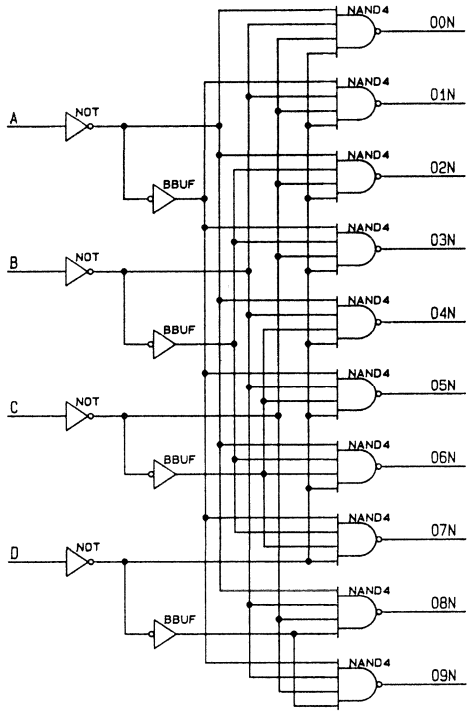
7442 Function Table:

7442 F unction Table

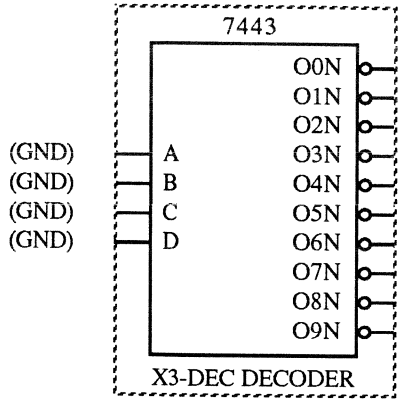
NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

H = high level
L = low level

7442 Logic Schematic:



7443 (Decoder)



Name: **7443** (Excess-3-to-Decimal Decoder)

Declaration: 7443(A,B,C,D,O9N,O8N,O7N,O6N,O5N, O4N, O3N,O2N,O1N,O0N)

EPLDs: EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

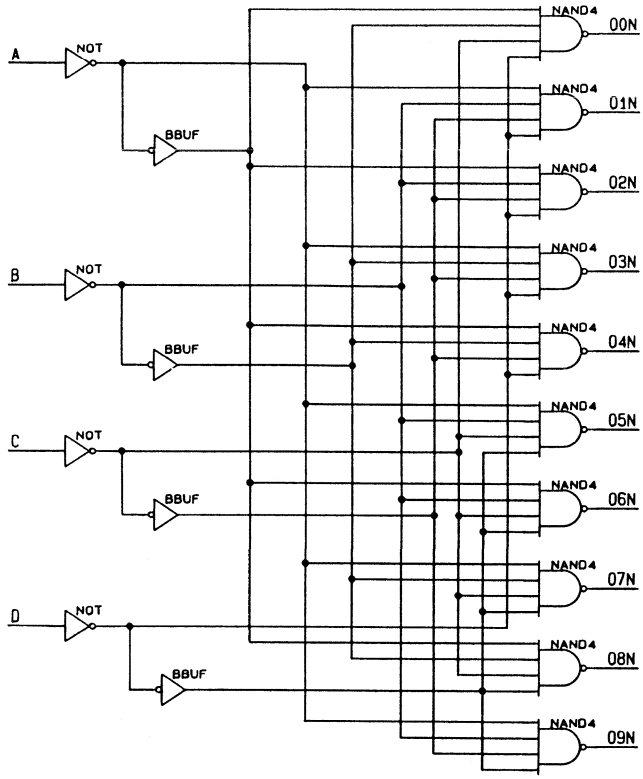
7443 Function Table:

7443 Function Table

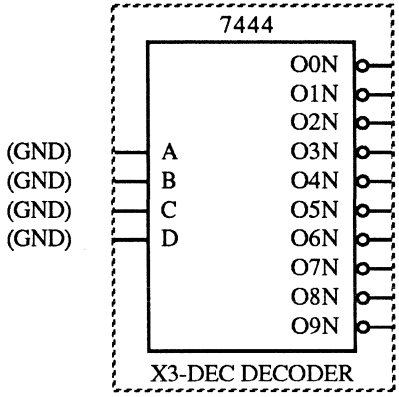
NO.	EXCESS-3 INPUTS				DECIMAL OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	H	H	L	H	H	H	H	H	H	H	H	H
1	L	H	L	L	H	L	H	H	H	H	H	H	H	H
2	L	H	L	H	H	H	L	H	H	H	H	H	H	H
3	L	H	H	L	H	H	H	L	H	H	H	H	H	H
4	L	H	H	H	H	H	H	H	L	H	H	H	H	H
5	H	L	L	L	H	H	H	H	H	L	H	H	H	H
6	H	L	L	H	H	H	H	H	H	H	L	H	H	H
7	H	L	H	L	H	H	H	H	H	H	H	L	H	H
8	H	L	H	H	H	H	H	H	H	H	H	H	L	H
9	H	H	L	L	H	H	H	H	H	H	H	H	H	L
I	H	H	L	H	H	H	H	H	H	H	H	H	H	H
N	H	H	H	L	H	H	H	H	H	H	H	H	H	H
V	H	H	H	H	H	H	H	H	H	H	H	H	H	H
A	L	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H
I	L	L	H	L	H	H	H	H	H	H	H	H	H	H
D														

H = high level
L = low level

7443 Logic Schematic:



7444 (Decoder)



Name: **7444** (Excess-3-to-Decimal Decoder)

Declaration: 7444(A,B,C,D,O9N,O8N,O7N,O6N,O5N, O4N, O3N,O2N,O1N,O0N)

EPLDs: EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

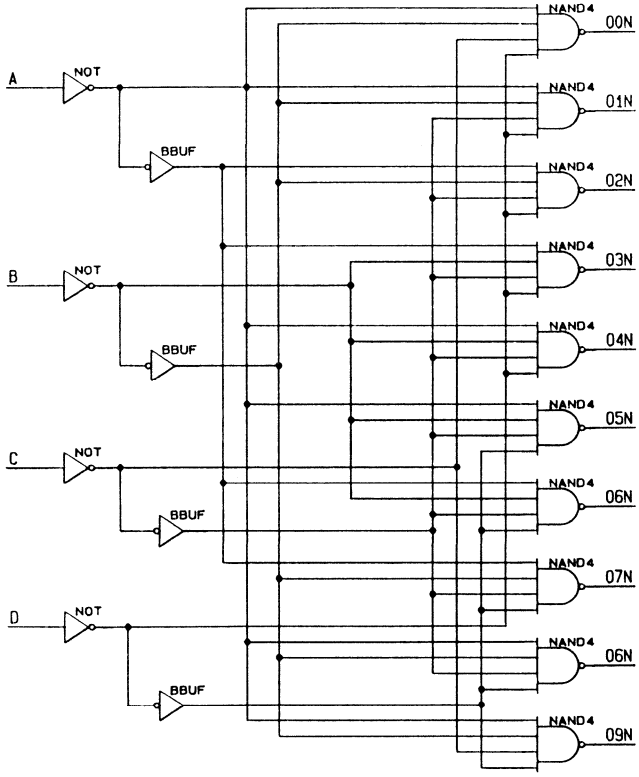
7444 Function Table:

7444 Function Table

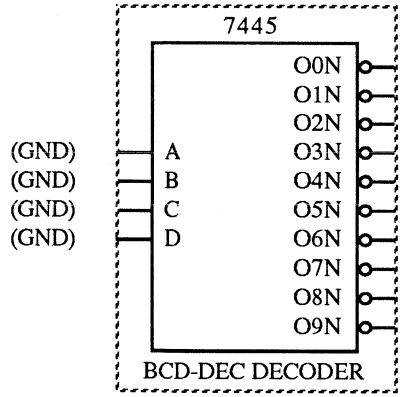
NO.	EXCESS 3-GRAY INPUTS				DECIMAL OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	H	L	L	H	H	H	H	H	H	H	H	H
1	L	H	H	L	H	L	H	H	H	H	H	H	H	H
2	L	H	H	H	H	H	L	H	H	H	H	H	H	H
3	L	H	L	L	H	H	H	L	H	H	H	H	H	H
4	H	H	L	L	H	H	H	H	L	H	H	H	H	H
5	H	H	L	L	H	H	H	H	H	L	H	H	H	H
6	H	H	L	H	H	H	H	H	H	H	L	H	H	H
7	H	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	H	H	L	H	H	H	H	H	H	H	H	L	H
9	H	L	H	L	H	H	H	H	H	H	H	H	H	L
I	H	L	H	H	H	H	H	H	H	H	H	H	H	H
N	H	L	L	H	H	H	H	H	H	H	H	H	H	H
V	H	L	L	L	H	H	H	H	H	H	H	H	H	H
A	L	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H
I	L	L	H	H	H	H	H	H	H	H	H	H	H	H
D														

H = high level
L = low level

7444 Logic Schematic:



7445 (Decoder)



Name: **7445** (BCD-to-Decimal Decoder)

Declaration: 7445(A,B,C,D,O9N,O8N,O7N,O6N,O5N, O4N,O3N,O2N,O1N,O0N)

EPLDs: EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

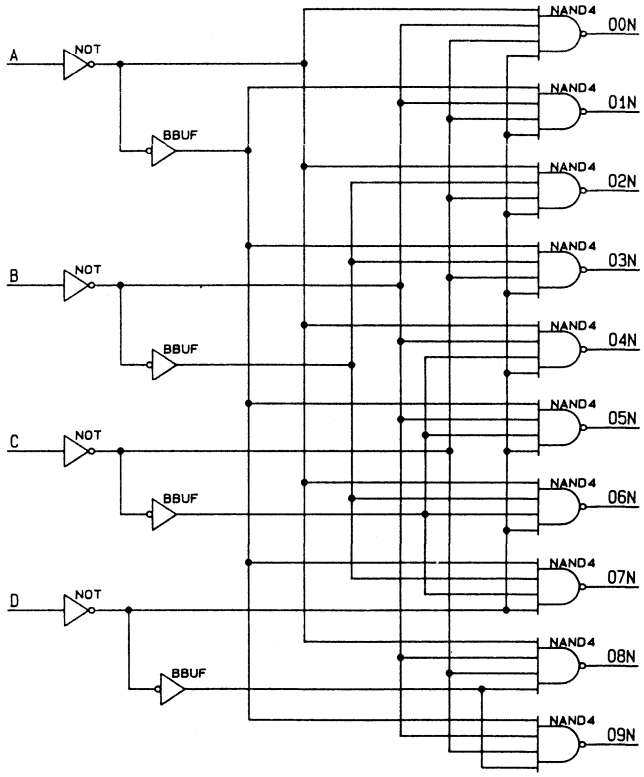
7445 Function Table:

7445 Function Table

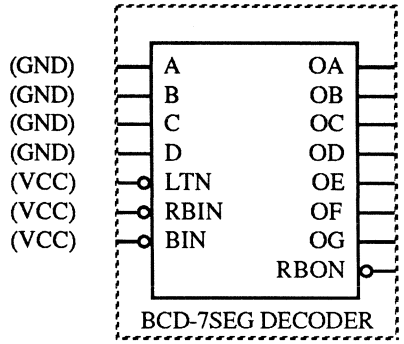
NO.	BCD INPUTS				DECIMAL OUTPUTS									
	D	B	C	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

H = high level
L = low level

7445 Logic Schematic:



7446 (Decoder)



Name: **7446** (BCD-to-7-Segment Decoder)

Declaration: 7446(A,B,C,D,LTN,RBIN,BIN,RBON,OG,OF, OE,OD,OC,OB,OA)

(Where: LT = Lamp Test; RBIN = Ripple Blank In; BIN = Blank In; RBON = Ripple Blank Out)

EPLDs: All

Default Signal Levels: GND — A, B, C, D
VCC — LTN, RBIN, BIN

7446 Function Table:

7446 Function Table

Decimal Or Function	INPUTS							OUTPUTS								Note
	LTN	RBIN	D	C	B	A	BIN	OA	OB	OC	OD	OE	OF	OG	RBON	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	H	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	H	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	H	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	H	
BI	X	X	X	X	X	X	X	L	H	H	H	H	H	H	X	2
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	L	3
LT	L	X	X	X	X	X	X	H	L	L	L	L	L	L	H	4

H = high level
L = low level
X = don't care

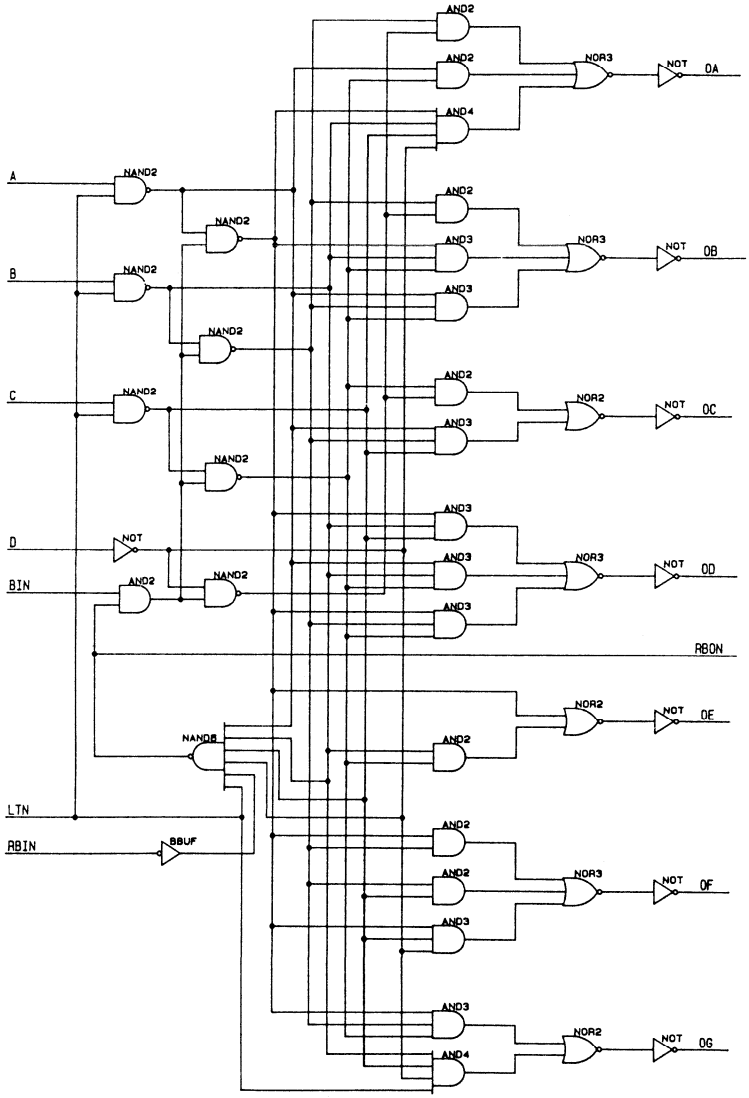
NOTES: 1. The blanking input (BIN) must be open or held at a high logic level when output functions 0 through 15 are desired. RBIN must be held high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BIN), all segment outputs are low regardless of the level of any other input.

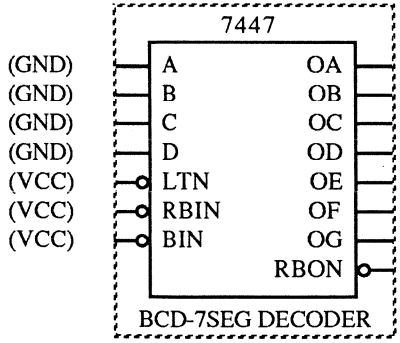
3. When RBIN, A, B, C, D are low and LTN is high, RBON goes low.

4. When LTN is held low, all outputs are high unless BIN is low.

7446 Logic Schematic:



7447 (Decoder)



Name: **7447** (BCD-to-7-Segment Decoder)

Declaration: 7447(A,B,C,D,LTN,RBIN,BIN,RBON,OG,OF, OE,OD,OC,OB,OA)

EPLDs: All

Default Signal Levels: GND — A, B, C, D
VCC — LTN, RBIN, BIN

7447 Function Table:

7447 Function Table

Decimal Or Function	INPUTS							OUTPUTS								Note
	LTN	RBIN	D	C	B	A	BIN	OA	OB	OC	OD	OE	OF	OG	RBON	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	H	
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	H	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	H	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	H	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	H	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	H	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	H	1
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	H	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	H	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	H	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	H	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	H	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	H	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	X	H	H	H	H	H	H	H	X	2
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	L	3
LT	L	X	X	X	X	X	X	L	L	L	L	L	L	L	H	4

H = high level
L = low level
X = don't care

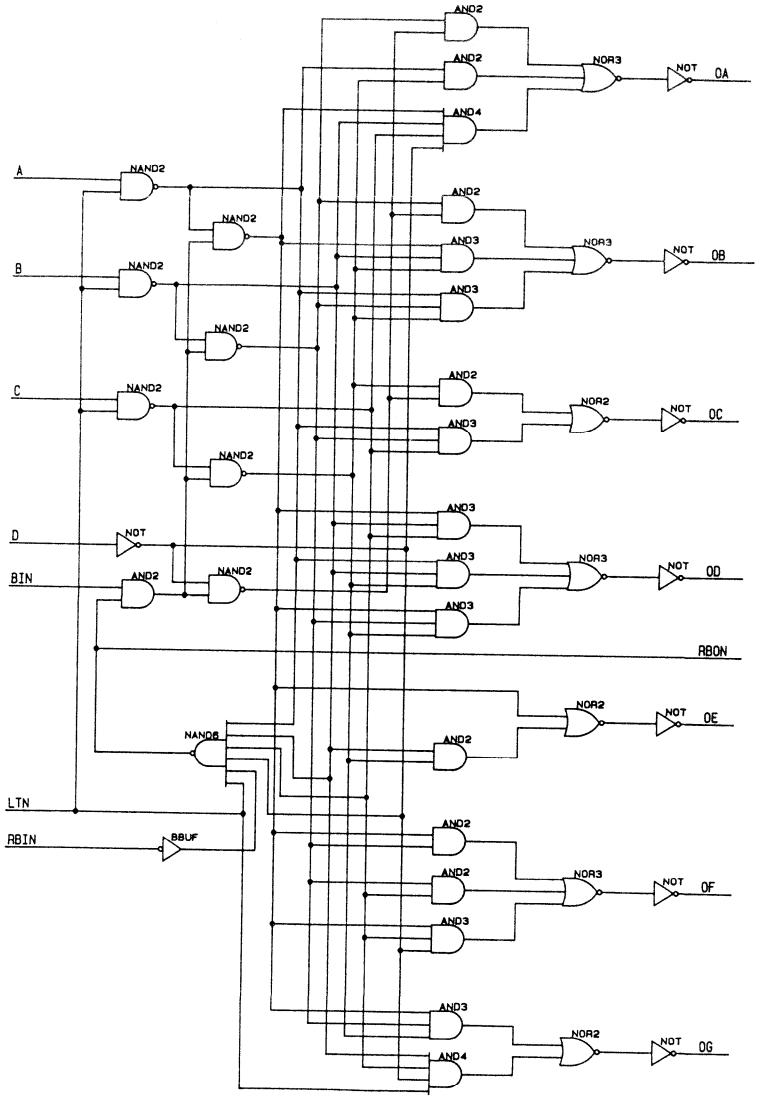
NOTES: 1. The blanking input (BIN) must be open or held at a high logic level when output functions 0 through 15 are desired. RBIN must be held high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BIN), all segment outputs are low regardless of the level of any other input.

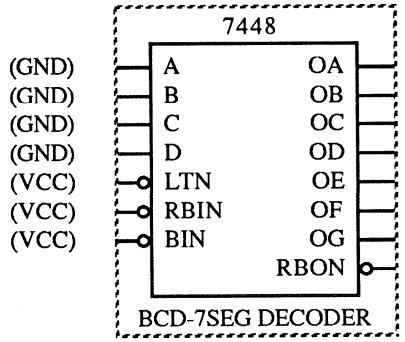
3. When RBIN, A, B, C, D are low and LTN is high, RBON goes low.

4. When LTN is held low, all outputs are high unless BIN is low.

7447 Logic Schematic:



7448 (Decoder)



Name: **7448** (BCD-to-7-Segment Decoder)

Declaration: 7448(A,B,C,D,LTN,RBIN,BIN,RBON,OG,OF, OE,OD,OC,OB,OA)

EPLDs: All

Default Signal Levels: GND — A, B, C, D
VCC — LTN, RBIN, BIN

7448 Function Table:

7448 Function Table

Decimal Or Function	INPUTS							OUTPUTS								Note
	LTN	RBIN	D	C	B	A	BIN	OA	OB	OC	OD	OE	OF	OG	RBON	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	H	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	H	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	H	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	H	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	X	2
RBI	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	H	4

H = high level
L = low level
X = don't care

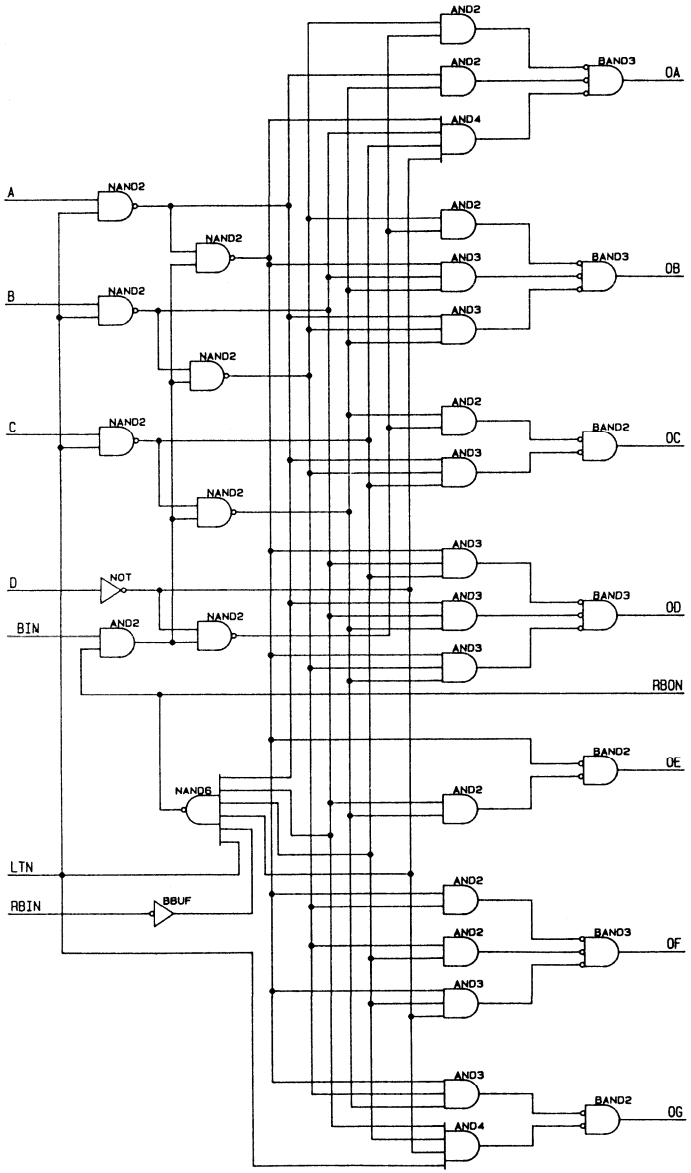
NOTES: 1. The blanking input (BIN) must be open or held at a high logic level when output functions 0 through 15 are desired. RBIN must be held high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BIN), all segment outputs are low regardless of the level of any other input.

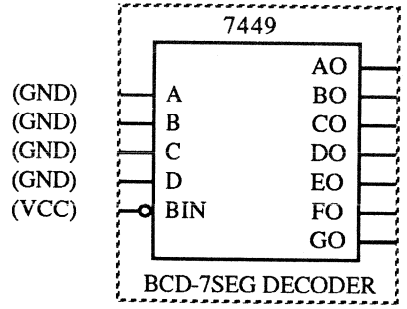
3. When RBIN, A, B, C, D are low and LTN is high, RBON goes low.

4. When LTN is held low, all outputs are high unless BIN is low.

7448 Logic Schematic:



7449 (Decoder)



Name: **7449** (BCD-To-7 Segment Decoder)

Declaration: 7449(A,B,C,D,BIN,GO,FO,EO,DO,CO, BO,AO)

EPLDs: All

Default Signal Levels: GND — A, B, C, D
VCC — BIN

7449 Function Table:

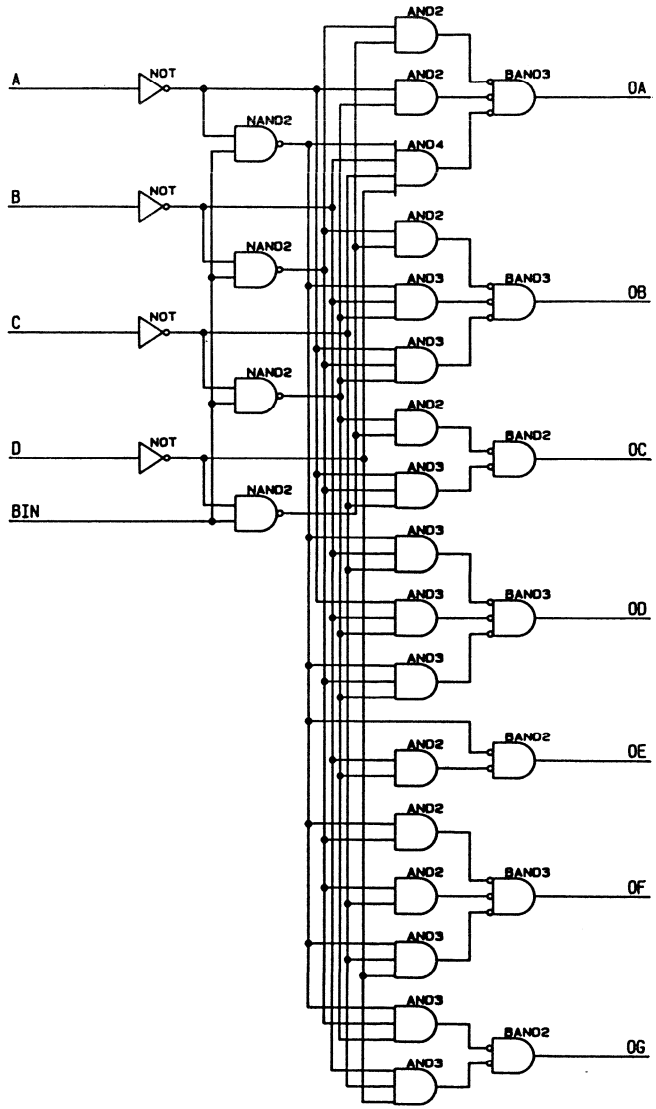
7449 Function Table

Decimal or Function	INPUTS					OUTPUTS							Note
	D	C	B	A	BIN	AO	BO	CO	DO	EO	FO	GO	
0	L	L	L	L	H	H	H	H	H	H	H	L	
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	1
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	L	L	L	L	L	L	L	L	2

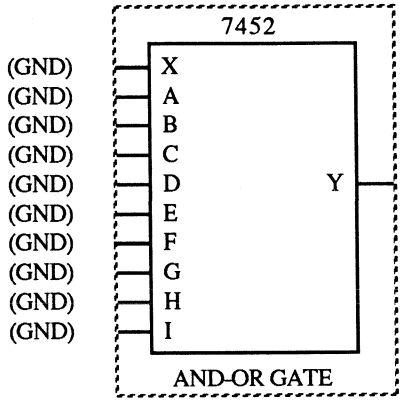
H = high level
L = low level
X = don't care
NOTES: 1. The blanking input (BIN) must be held at a high logic level when output functions 0 through 15 are desired.

2. When a low logic level is applied directly to the blanking input (BIN), all segment outputs are low regardless of the level of any other input.

7449 Logic Schematic:



7452 (AND-OR Gate)



Name: **7452** (AND-OR Gate)

Declaration: 7452(X,A,B,C,D,E,F,G,H,I,Y)

EPLDs: All

Default Signal Levels: GND — all input pins

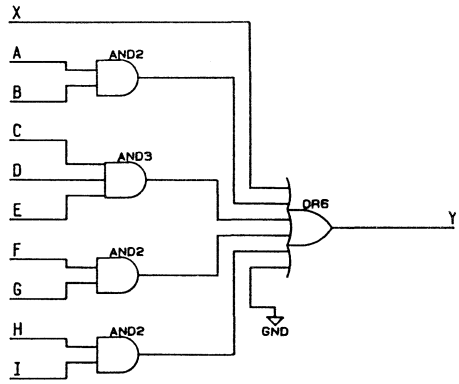
7452 Function Table:

7452 Function Table

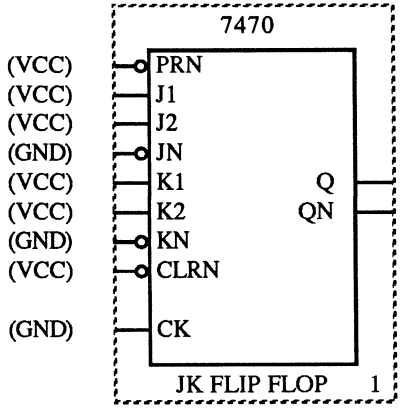
INPUTS										OUTPUT
X	A	B	C	D	E	F	G	H	I	Y*
H	X	X	X	X	X	X	X	X	X	H
X	H	H	X	X	X	X	X	X	X	H
X	X	X	H	H	H	X	X	X	X	H
X	X	X	X	X	X	H	H	X	X	H
X	X	X	X	X	X	X	X	H	H	H

*All other combinations of inputs cause Y to go low.
H = high level
L = low level
X = don't care

7452 Logic Schematic:



7470 (Register)



Name: **7470** (AND-Gated J-K Flipflop With Preset and Clear)

Declaration: 7470(PRN,J1,J2,JN,K1,K2,KN, CLRN,CK,QN,Q)

EPLDs: EP310, EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — JN, KN, CK
VCC — J1, J2, K1, K2, CLRN

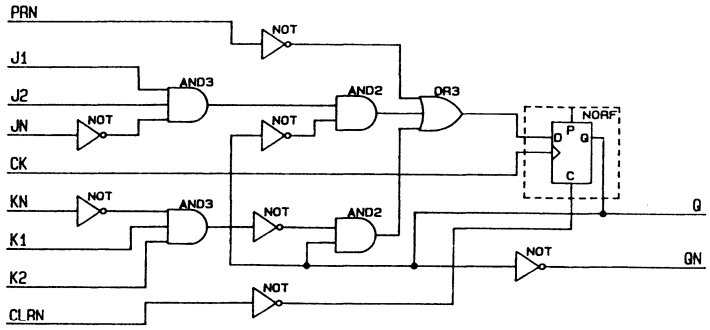
7470 Function Table:

7470 Function Table

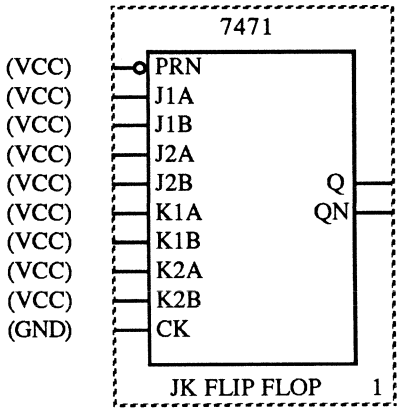
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	⌐	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	ILLEGAL	
H	H	⌐	L	L	Qo	$\overline{Qo}$
H	H	⌐	H	L	H	L
H	H	⌐	L	H	L	H
H	H	⌐	H	H	TOGGLE	
H	H	X	X	X	Qo	$\overline{Qo}$

X = don't care
H = high level
L = low level
J = J1 * J2 * J
K = K1 * K2 * $\overline{K}$
Qo = value of Q before clock pulse
⌐ = transition from low to high
If inputs J and K are not used, they must be GND.

7470 Logic Schematic:



7471 (Register)



Name: **7471** (J-K Flipflop With Preset)

Declaration: 7471(PRN,J1A,J1B,J2A,J2B,K1A,K1B, K2A,K2B,CK,QN,Q)

EPLDs: All

Default Signal Levels: GND — CK
VCC — PRN, J1A,J1B, J2A, J2B, K1A, K1B, K2A, K2B

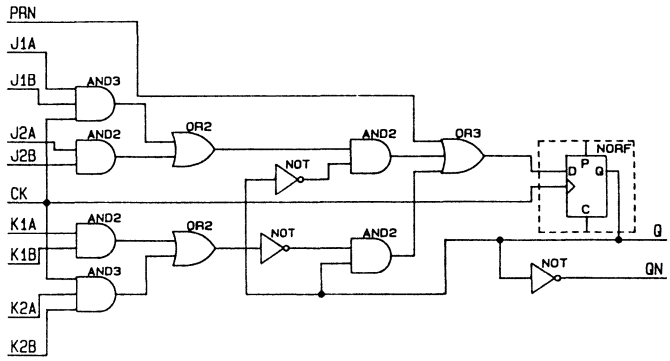
7471 Function Table:

7471 Function Table

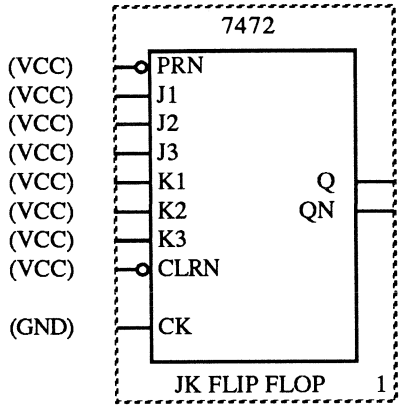
INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\overline{Q}$
L	⌐	X	X	H	L
H	⌐	L	L	Qo	$\overline{Qo}$
H	⌐	H	L	H	L
H	⌐	L	H	L	H
H	⌐	H	H	TOGGLE	

J = (J1A * J1B) + (J2A * J2B)
K = (K1A * K1B) + (K2A * K2B)
Qo = value of Q before clock pulse
⌐ = transition from low to high
H = high level
L = low level
X = don't care

7471 Logic Schematic:



7472 (Register)



Name: **7472** (AND-Gated Flipflop With Preset and Clear)

Declaration: 7472(PRN,J1,J2,J3,K1,K2,K3,CLRN,CK, QN,Q)

EPLDs: EP310, EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — CK
VCC — PRN, J1, J2, J3, K1, K2, K3, CLRN

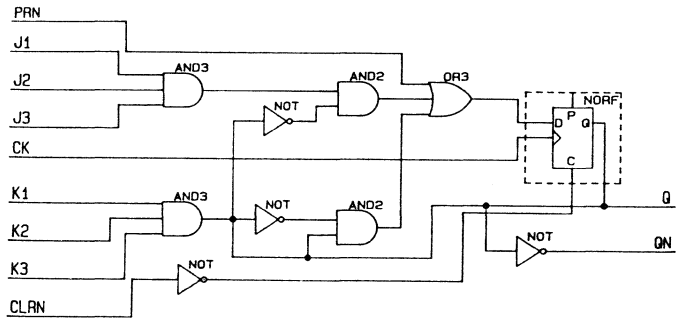
7472 Function Table:

7472 Function Table

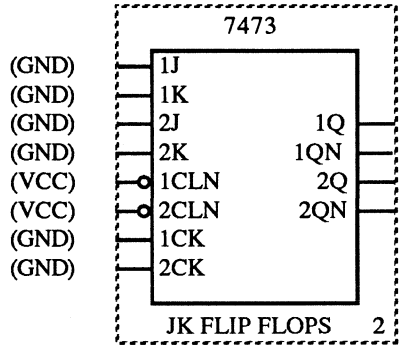
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	⌐	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	ILLEGAL	
H	H	⌐	L	L	Qo	$\overline{Qo}$
H	H	⌐	L	H	L	H
H	H	⌐	H	L	H	L
H	H	⌐	H	H	TOGGLE	

J = J1 * J2 * J3
K = K1 * K2 * K3
Qo = value of Q before clock pulse
⌐ = transition from low to high
H = high level
L = low level
X = don't care

7472 Logic Schematic:



7473 (Register)



Name: **7473** (Dual J-K Flipflop With Clear)

Declaration: 473(1J,1K,2J,2K,1CLN,2CLN,1CK,2CK, 2QN, 2Q,1QN,1Q)

EPLDs: EP310, EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — 1J, 1K, 2J, 2K, 1CK, 2CK
VCC — 1CLN, 2CLN

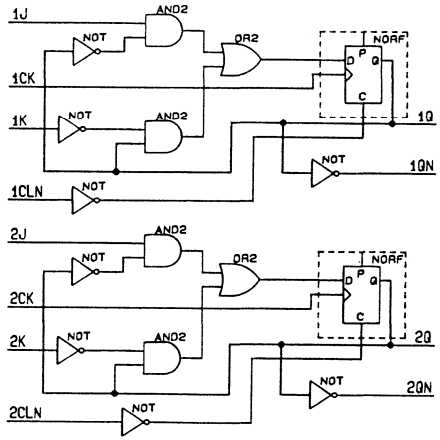
7473 Function Table:

7473 Function Table

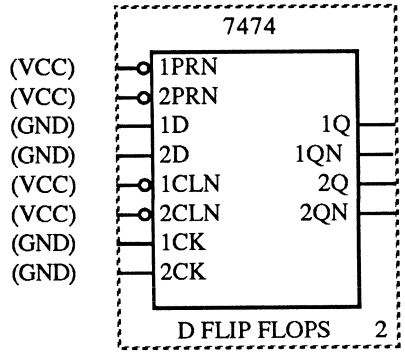
INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⌐	L	L	Qo	$\overline{Qo}$
H	⌐	H	L	H	L
H	⌐	L	H	L	H
H	⌐	H	H	TOGGLE	

Qo = value of Q before clock pulse
⌐ = transition from low to high
H = high level
L = low level
X = don't care

7473 Logic Schematic:



7474 (Register)



Name: **7474** (Dual D-Type Flipflop With Preset and Clear)

Declaration: 7474(1PRN,2PRN,1D,2D,1CLN,2CLN,1CK, 2CK,2QN,2Q,1QN,1Q)

EPLDs: All

Default Signal Levels: GND — 1D, 2D, 1CK, 2CK
VCC — 1PRN, 2PRN, 1CLN, 2CLN

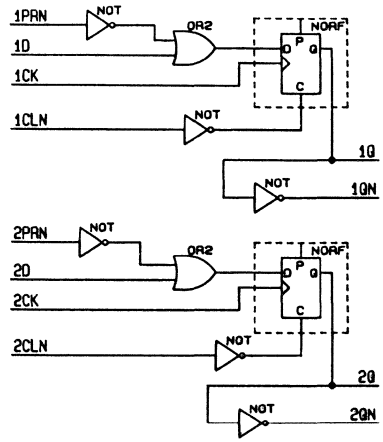
7474 Function Table:

7474 Function Table

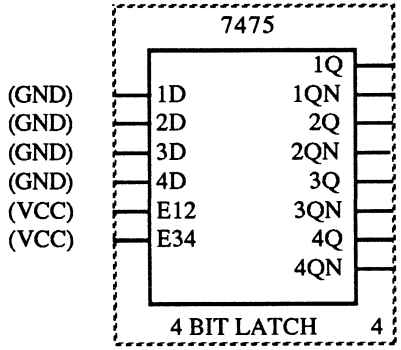
INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	⌐	X	H	L
H	L	X	X	L	H
L	L	X	X	ILLEGAL	
H	H	⌐	L	L	H
H	H	⌐	H	H	L
H	H	⌐	X	Qo	$\overline{Qo}$

Qo = value of Q before clock pulse
⌐ = transition from low to high
H = high level
L = low level
X = don't care

7474 Logic Schematic:



7475 (Latch)



Name: **7475** (4-Bit Bi-Stable Latch)

Declaration: 7475(1D,2D,3D,4D,E12,E34,4QN,4Q, 3QN,3Q, 2QN,2Q,1QN,1Q)

EPLDs: All

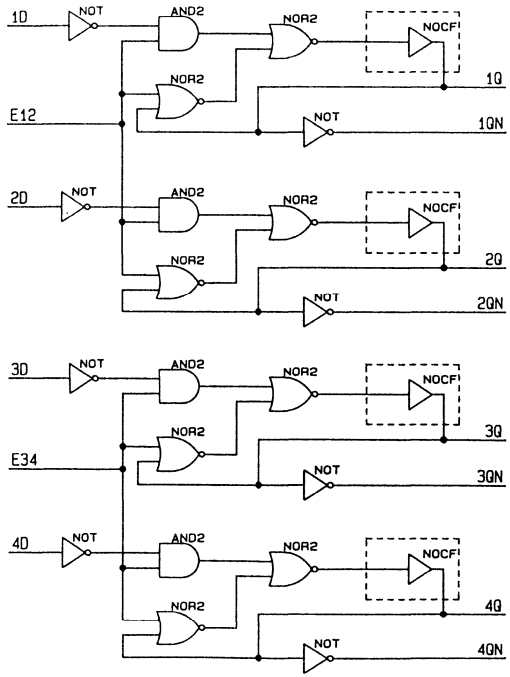
Default Signal Levels: GND — 1D, 2D, 3D, 4D
VCC — E12, E34

7475 Function Table:

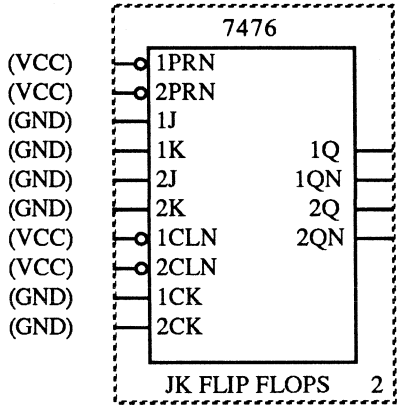
7475 Function Table

INPUTS		OUTPUTS		Qo = level of Q before G goes from high to low H = high level L = low level X = don't care
D	G	Q	$\overline{Q}$	
X	X	L	H	
L	L	H	L	
H	L	Qo	$\overline{Qo}$	
L	H			
H	H			

7475 Logic Schematic:



7476 (Register)



Name: **7476** (Dual J-K Flipflop With Synchronous Preset and Asynchronous Clear)

Declaration: 7476(1PRN,2PRN,1J,1K,2J,2K,1CLN,2CLN, 1CK,2CK,2QN,2Q,1QN,1Q)

EPLDs: EP310, EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

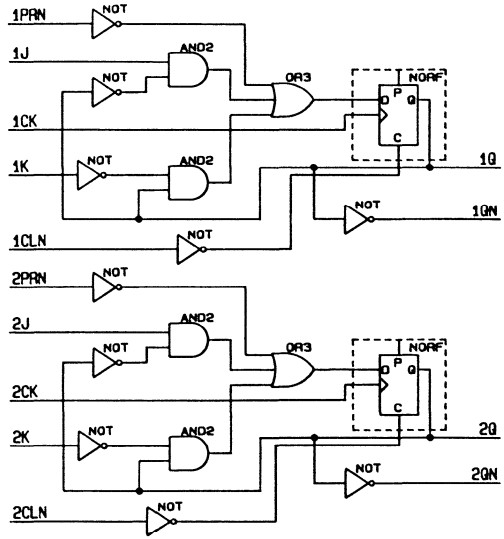
Default Signal Levels: GND — 1J, 1K, 2J, 2K, 1CK, 2CK
VCC — 1PRN, 2PRN, 1CLN, 2CLN

7476 Function Table:

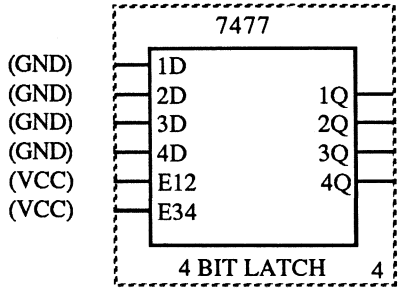
7476 Function Table

INPUTS					OUTPUTS		Qo = value of Q before last clock pulse ⌐ = transition from low to high H = high level L = low level X = don't care
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$	
L	H	⌐	X	X	H	L	
H	L	X	X	X	L	H	
L	L	X	X	X	ILLEGAL		
H	H	⌐	L	L	Qo	$\overline{Qo}$	
H	H	⌐	H	L	H	L	
H	H	⌐	L	H	L	H	
H	H	⌐	H	H	TOGGLE		

7476 Logic Schematic:



7477 (Latch)



Name: **7477** (4-Bit Bi-Stable Latch)

Declaration: 7477(1D,2D,3D,4D,E12,E34,4Q,3Q,2Q,1Q)

EPLDs: All

Default Signal Levels: GND — 1D, 2D, 3D, 4D
VCC — E12, E34

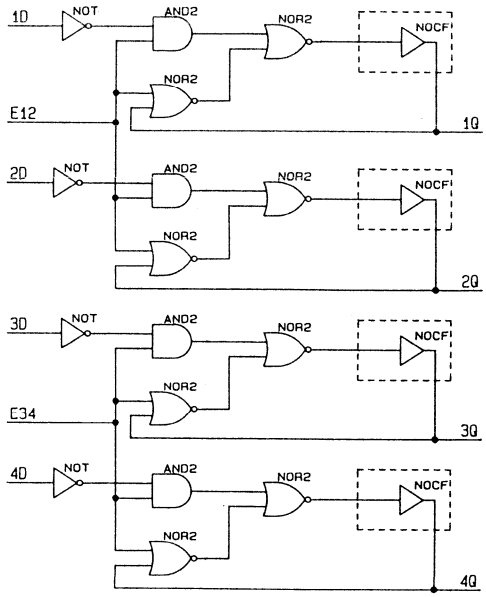
Function Table:

7477 Function Table

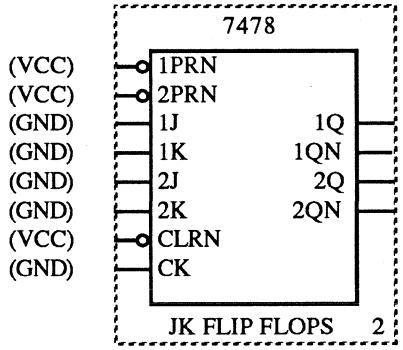
INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qo	$\overline{Qo}$

Qo = level of Q before G goes from high to low
H = high level
L = low level
X = don't care

7477 Logic Schematic:



7478 (Register)



Name: **7478** (Dual J-K Flipflop With Synchronous Preset, Common Clear, and Common Clock)

Declaration: 7478(1PRN,2PRN,1J,1K,2J,2K,CLRN,CK, 2QN,2Q,1QN,1Q)

EPLDs: EP310, EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

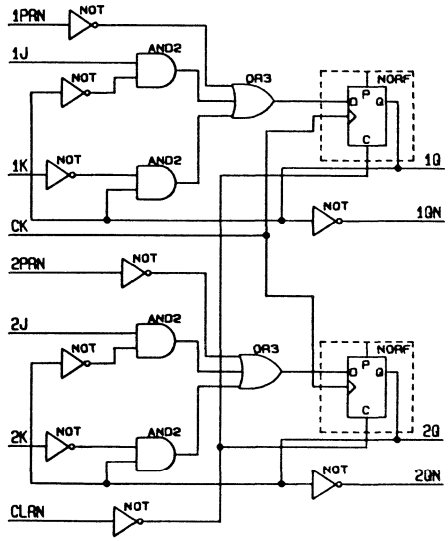
Default Signal Levels: GND — 1J, 1K, 2J, 2K
VCC — 1PRN, 2PRN, CLRN

7478 Function Table:

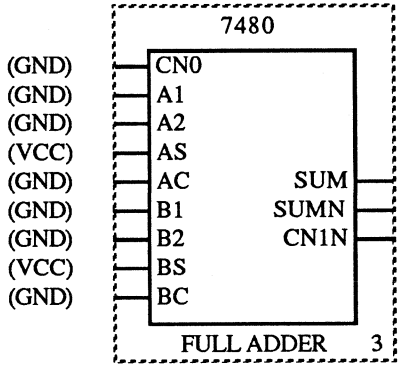
7478 Function Table

INPUTS					OUTPUTS		Qo = value of $\overline{Q}$ before last clock pulse ⌐ = transition from low to high H = high level L = low level X = don't care
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$	
L	H	⌐	X	X	H	L	
H	L	X	X	X	L	H	
L	L	X	X	X	ILLEGAL		
H	H	⌐	L	L	Qo	$\overline{Qo}$	
H	H	⌐	H	L	H	L	
H	H	⌐	L	H	L	H	
H	H	⌐	H	H	TOGGLE		
H	H	L	X	X	Qo	$\overline{Qo}$	

7478 Logic Schematic:



7480 (Full Adder)



Name: **7480** (Gated Full Adder)

Declaration: 7480(CN0,A1,A2,AS,AC,B1,B2,BS,BC, CN1N, SUMN,SUM)

EPLDs: All

Default Signal Levels: GND — CN0, A1, A2, AC, B1, B2, BC
VCC — AS, BS

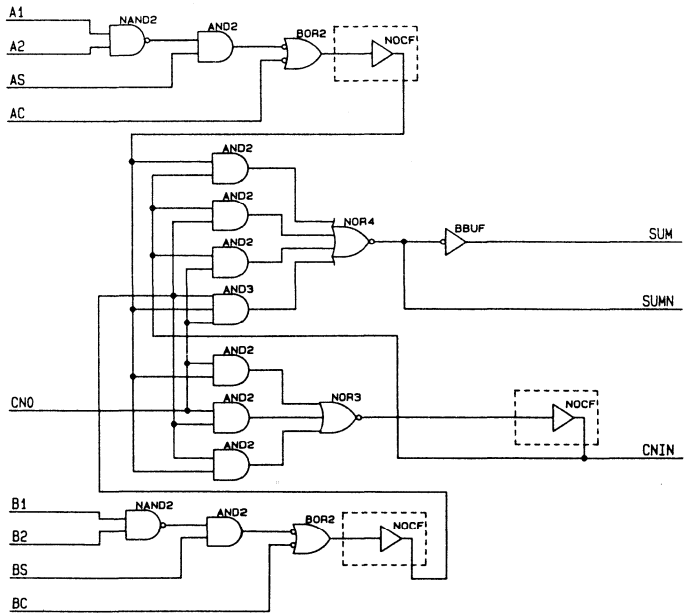
7480 Function Table:

7480 Function Table

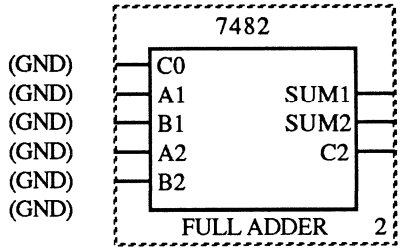
INPUTS			OUTPUTS		
CN0	A	B	CN1N	SUM	SUMN
L	L	L	H	L	H
L	L	H	H	H	L
L	H	L	H	H	L
L	H	H	L	L	H
H	L	L	H	H	L
H	L	H	L	L	H
H	H	L	L	L	H
H	H	H	L	H	L

H = high level
L = low level
$A = \overline{AC} + \overline{AS} + A1 * A2$
$B = \overline{BC} + \overline{BS} + B1 * B2$

7480 Logic Schematic:



7482 (Full Adder)



Name: **7482** (2-Bit Binary Full Adder)

Declaration: 7482(C0,A1,B1,A2,B2,C2,SUM2,SUM1)

EPLDs: All

Default Signal Levels: GND — all input pins

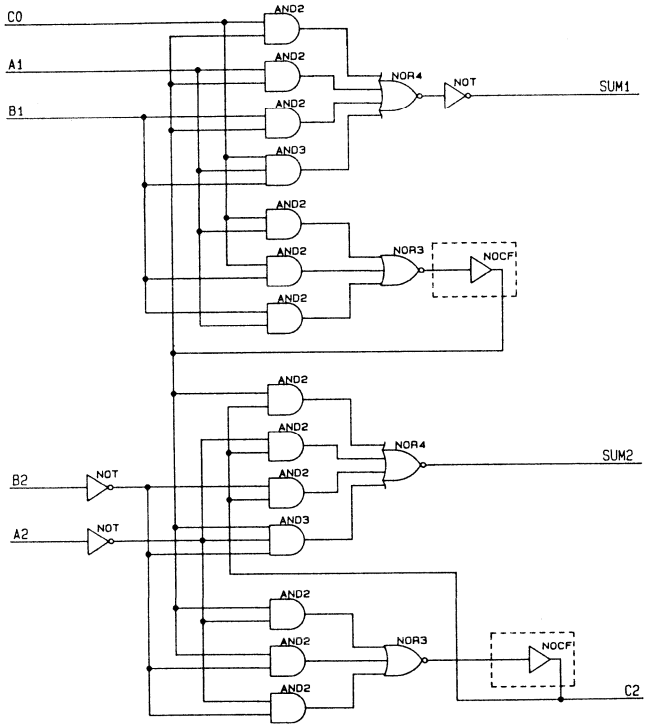
7482 Function Table:

7482 Function Table

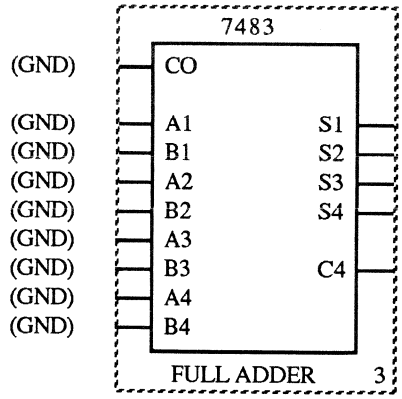
INPUTS				OUTPUTS					
				WHEN C0 = L			WHEN C0 = H		
A1	B1	A2	B2	SUM1	SUM2	C2	SUM1	SUM2	C2
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level
L = low level

7482 Logic Schematic:



7483 (Full Adder)



Name: **7483** (4-Bit Full Adder)

Declaration: 7483(C0,A1,B1,A2,B2,A3,B3,A4,B4,C4, S4,S3,S2,S1)

EPLDs: All

Default Signal Levels: GND — all input pins

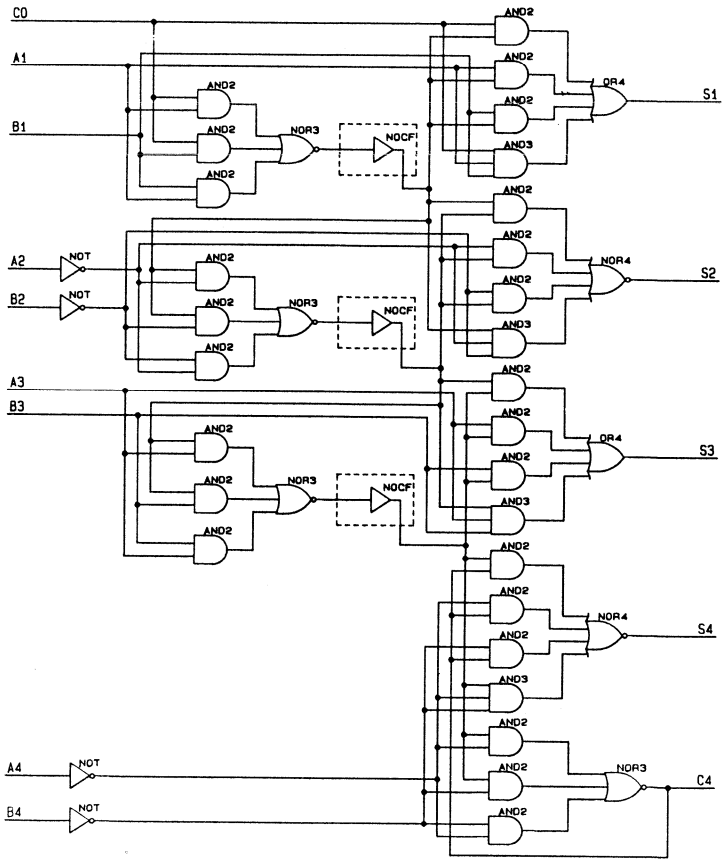
7483 Function Table:

7483 Function Table

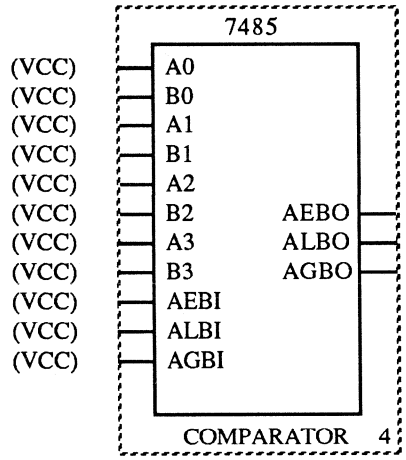
INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	S1 / S3	S2 / S4	C2 / C4	S1 / S3	S2 / S4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level
L = low level
Input conditions at A1, B1, A2, B2, C0 are used to determine outputs S1 and S2 and the value of the internal carry C2. The values at C2, A3, B3, A4, B4 are then used to determine outputs S3, S4, C4.

7483 Logic Schematic:



7485 (Comparator)



Name: **7485** (4-Bit Magnitude Comparator)

Declaration: 7485(A0,B0,A1,B1,A2,B2,A3,B3,AEBI,ALBI, AGBI,AGBO,ALBO,AEBO)

EPLDs: All

Default Signal Levels: VCC — all input pins

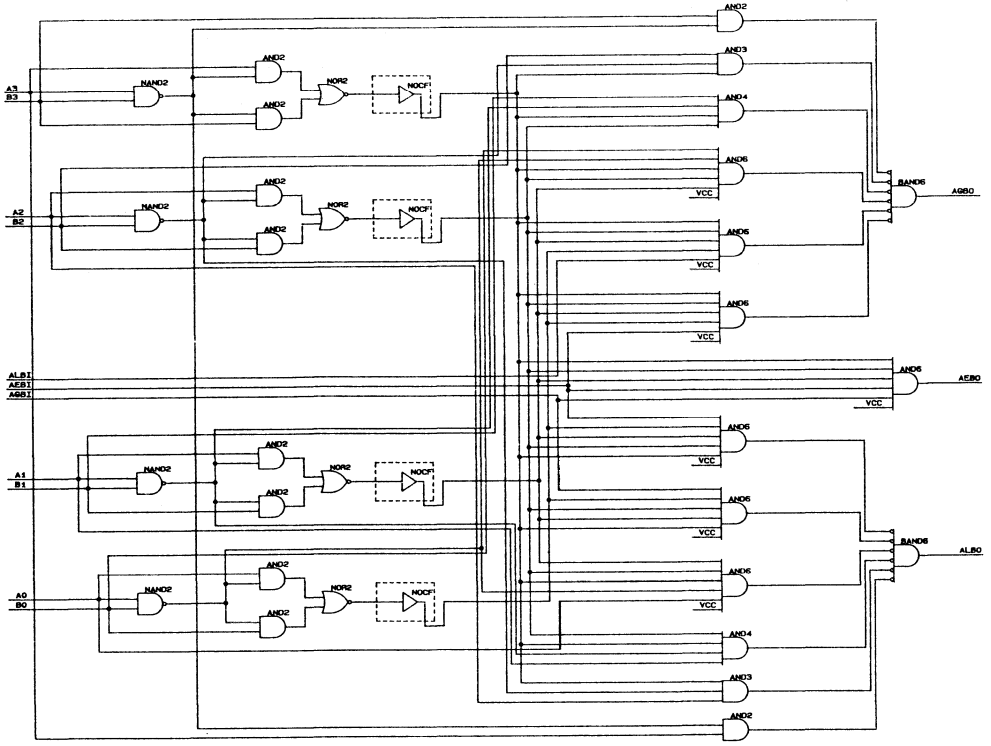
7485 Function Table:

7485 Function Table

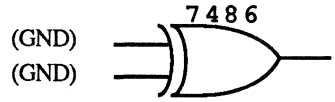
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B2	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

H = high level L = low level X = don't care

7485 Logic Schematic:



7486 (SSI Function)



Name: **7486** (XOR)

Declaration: 7486(A,B,OUT)

EPLDs: All

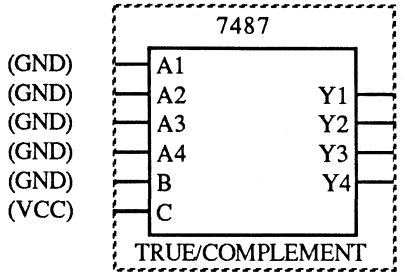
Default Signal Levels: GND — all input pins

Function Table:

7486 Function Table

INPUTS		OUTPUT
A	B	
0	0	0
0	1	1
1	0	1
1	1	0

7487 (True/Complement I/O Element)



Name: **7487** (4-Bit True/Complement I/O Element)

Declaration: 7487(A1,A2,A3,A4,B,C,Y4,Y3,Y2,Y1)

EPLDs: All

Default Signal Levels: GND — A1, A2, A3, A4, B
VCC — C

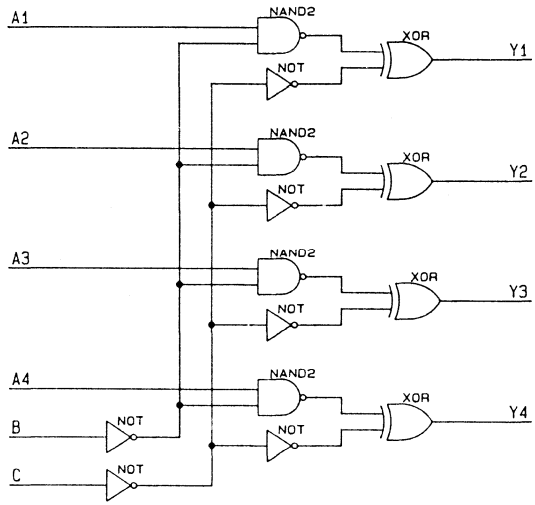
7487 Function Table:

7487 Function Table

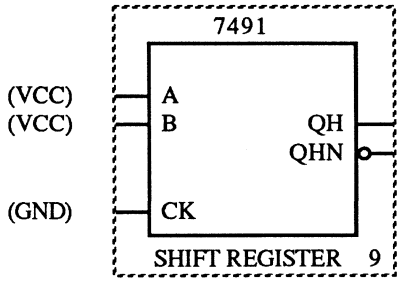
CONTROL INPUTS		OUTPUTS			
A	B	Y1	Y2	Y3	Y4
L	L	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$
L	H	A1	A2	A3	A4
H	L	H	H	H	H
H	H	L	L	L	L

H = high level L = low level
A1,A2,A3,A4 = level of the respective A inputs

7487 Logic Schematic:



7491 (Shift Register)



Name: **7491** (Serial-In Serial-Out Shift Register)

Declaration: 7491(A,B,CK,QHN,QH)

EPLDs: All

Default Signal Levels: GND — CK
VCC — A, B

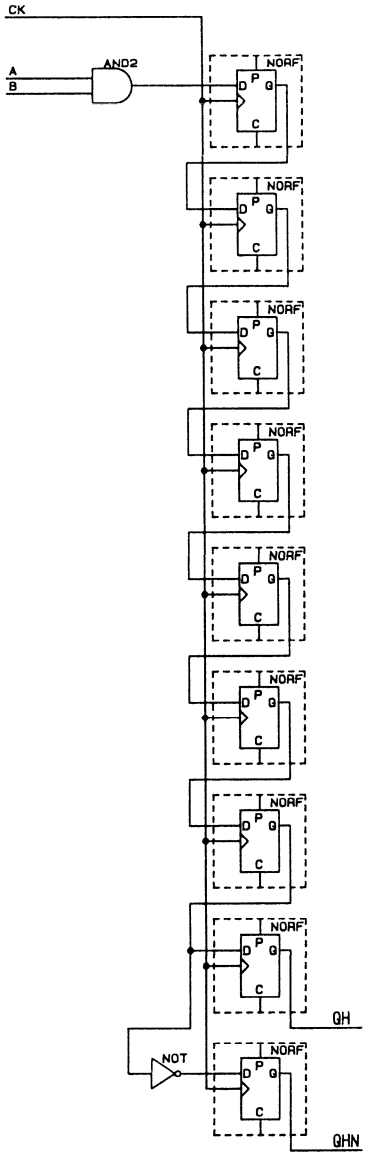
Function Table:

7491 Function Table

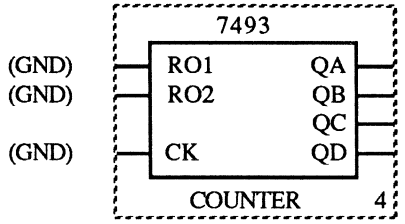
INPUTS AT t_n		OUTPUTS AT t_{n+8}	
A	B	Q_H	$\overline{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

H = high L = low X = don't care
t_n = reference bit time, clock low
t_{n+8} = bit time after 8 low-to-high clock transitions

7491 Logic Schematic:



7493 (Counter)



Name: **7493** (4-Bit Binary Counter)

Declaration: 7493(RO1,RO2,CK,QD,QC,QB, QA)

EPLDs: EP310, EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

7493 Function Table:

7493 Function Table (Count Sequence)

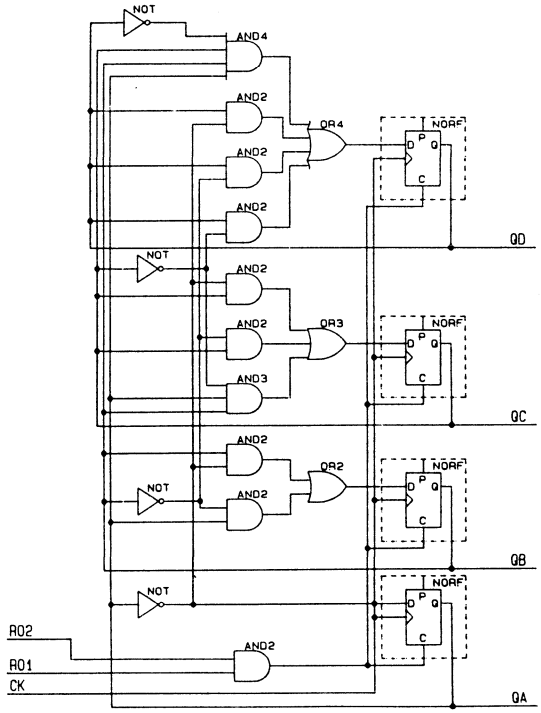
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = high level
L = low level

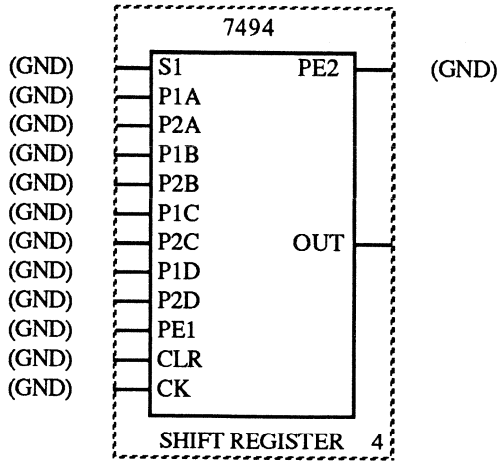
7493 Function Table (Reset/Count)

RESET INPUTS		OUTPUT			
$R_{O(1)}$	$R_{O(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

7493 Logic Schematic:



7494 (Shift Register)



Name: **7494** (4-Bit Shift Register With Synchronous Preset and Asynchronous Clear)

Declaration: 7494(S1,P1A,P2A,P1B,P2B,P1C,P2C, P1D,P2D,PE1,CLR,CK,OUT,PE2)

EPLDs: EP310, EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

7494 Function Table:

7494 Function Table

INTERNAL PRESETS				INPUTS			INTERNAL OUTPUTS			OUTPUT
A	B	C	D	CLEAR	CLOCK	SI	Q_A	Q_B	Q_C	Q_D
H	H	H	H	H	X	X	L	L	L	L
L	L	L	L	L	⌐	X	H	H	H	H
H	H	H	H	L	L	X	Q_{Ao}	Q_{Bo}	Q_{Co}	Q_{Do}
L	H	L	H	L	⌐	X	H	Q_{An}	H	Q_{Cn}
H	H	H	H	L	⌐	L	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	H	H	L	⌐	H	H	Q_{An}	Q_{Bn}	Q_{Cn}

H = high level L = low level X = don't care

⌐ = transition from low to high

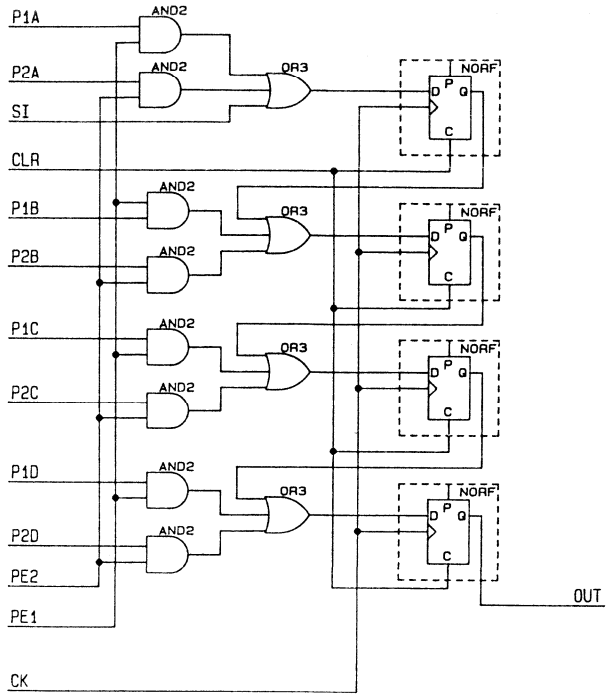
$Q_{Ao}, Q_{Bo}, Q_{Co}, Q_{Do}$ = level of the respective output before the indicated staedy-state condition

$Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}$ = level of the respective output before the last ⌐ of the clock

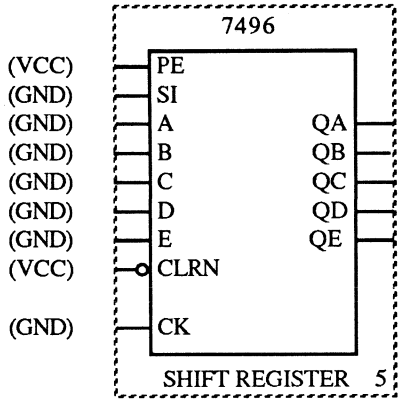
Preset Function Table
(Bit A, typical of all)

PRESET INPUTS				INTERNAL PRESET A
PE1	P1A	PE2	P2A	
L	X	L	X	H (INACTIVE)
L	X	X	L	H (INACTIVE)
X	L	L	X	H (INACTIVE)
X	L	X	L	H (INACTIVE)
H	H	X	X	L (ACTIVE)
X	X	H	H	L (ACTIVE)

7494 Logic Schematic:



7496 (Shift Register)



Name: **7496** (5-Bit Shift Register)

Declaration: 7496(PE,SI,A,B,C,D,E,CLRN,CK,QE,QD, QC,QB,QA)

EPLDs: EP310, EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — SI, A, B, C, D, E, CK
VCC — PE, CLRN

7496 Function Table:

7496 Function Table

INPUTS									OUTPUTS				
CLEAR	PRESET ENABLE	PRESET A	B	C	D	E	CLOCK	SI	Q_A	Q_B	Q_C	Q_D	Q_E
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	⌐	X	H	H	H	H	H
H	X	X	X	X	X	X	L	X	Q_{Ao}	Q_{Bo}	Q_{Co}	Q_{Do}	Q_{Eo}
H	H	H	L	H	L	H	⌐	X	H	Q_{An}	H	Q_{Cn}	H
H	H	L	H	L	H	L	⌐	L	L	H	Q_{Bn}	H	Q_{Dn}
H	L	X	X	X	X	X	⌐	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	⌐	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

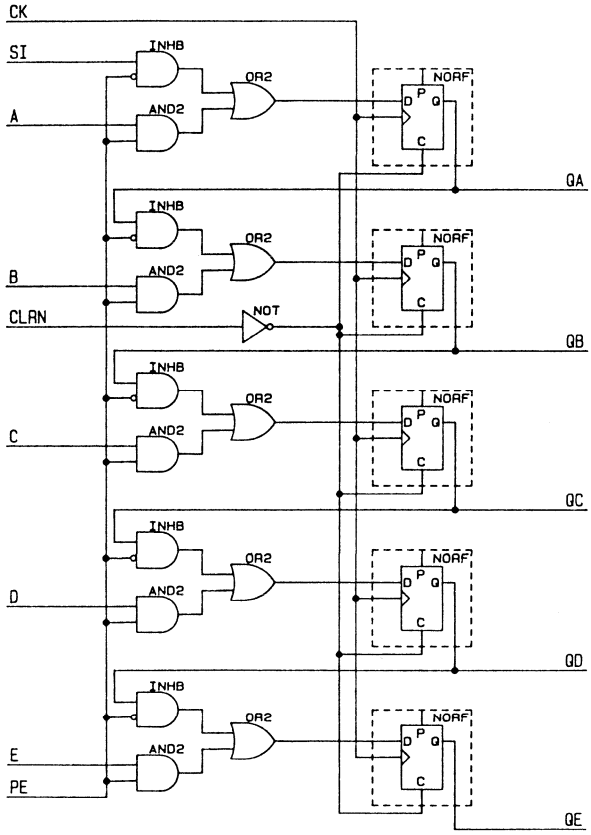
H = high level L = low level X = don't care

⌐ = transition from low to high

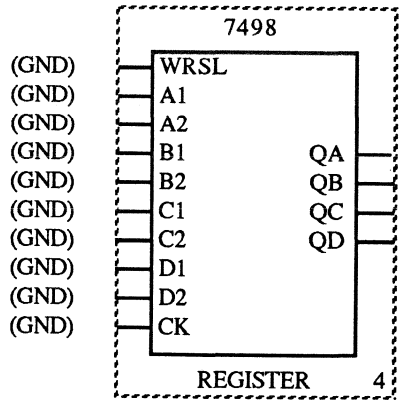
$Q_{Ao}, Q_{Bo}, Q_{Co}, Q_{Do}$ = level of the respective output before the indicated steady-state condition

$Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}$ = level of the respective output before the last ⌐ of the clock

7496 Logic Schematic:



7498 (Storage Register)



Name: **7498** (4-Bit Data Selector/Storage Register)

Declaration: 7498(WRSL,A1,A2,B1,B2,C1,C2,D1,D2, CK,QD,QC,QB,QA)

EPLDs: All

Default Signal Levels: GND — all input pins

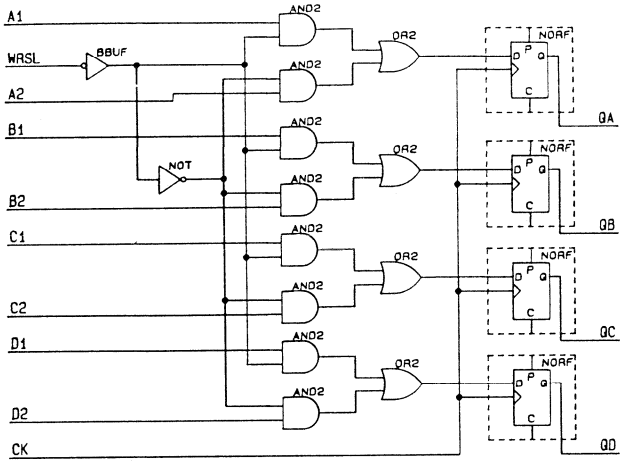
Function Table:

7498 Function Table

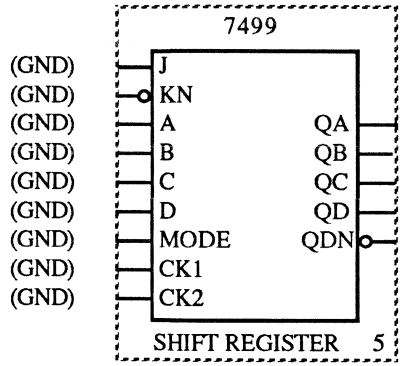
INPUTS										OUTPUTS			
CK	WRSL	A1	B1	C1	D1	A2	B2	C2	D2	Q_A	Q_B	Q_C	Q_D
⌐¬	L	a1	b1	c1	d1	X	X	X	X	a1	b1	c1	d1
⌐¬	H	X	X	X	X	a2	b2	c2	d2	a2	b2	c2	d2

H = high level L = low level X = don't care
⌐¬= transition from low to high

7498 Logic Schematic:



7499 (Shift Register)



Name: **7499** (4-Bit Shift Register With JK Serial and Parallel Inputs-Parallel Out)

Declaration: 7499(J,KN,A,B,C,D,MODE,CK1,CK2, QDN,QD,QC,QB,QA)

EPLDs: EP600, EP610, EP900, EP910, EP1800, EPB1400

Default Signal Levels: GND — all input pins

7499 Function Table:

7499 Function Table

INPUTS									OUTPUTS				
MODE	CLOCKS CK2	CLOCKS CK1	SERIAL J	SERIAL $\overline{K}$	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D	$\overline{Q_D}$
H	H	X	X	X							HOLD		
H	↓	X	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	↓	X	X	X	Q_B*	Q_C*	Q_D*	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d	$\overline{d}$
L	X	H	X	X							HOLD		
L	X	↓	L	H					Q_{Ao}	Q_{Ao}	Q_{Bn}	Q_{Cn}	$\overline{Q_{Cn}}$
L	X	↓	L	L					L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q_{Cn}}$
L	X	↓	H	H					H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q_{Cn}}$
L	X	↓	H	L					$\overline{Q_{An}}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q_{Cn}}$
↑	L	L	X	X							HOLD		

H = high level L = low level X = don't care

↑ = transition from low to high

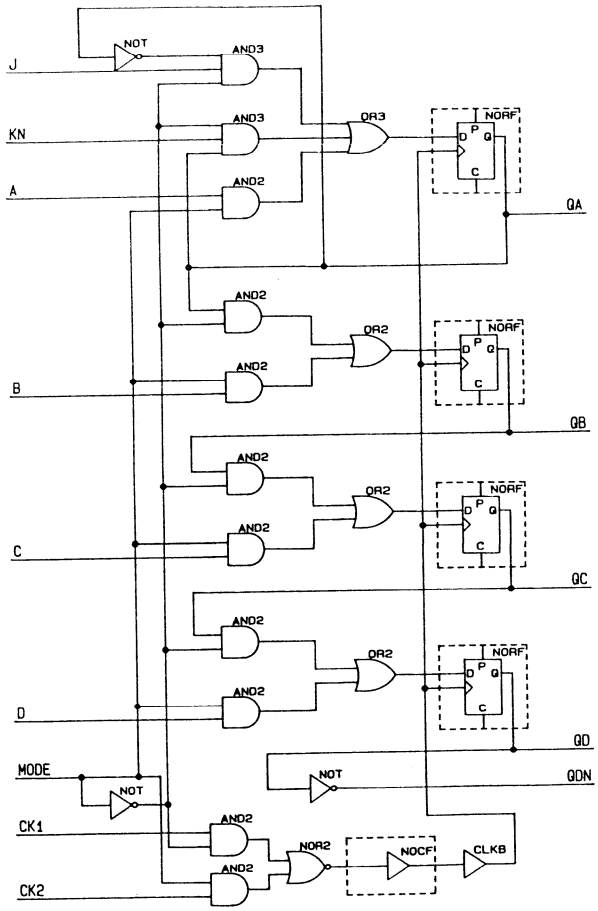
↓ = transition from high to low

$Q_{Ao}, Q_{Bo}, Q_{Co}, Q_{Do}$ = level of the respective output before the indicated steady-state condition

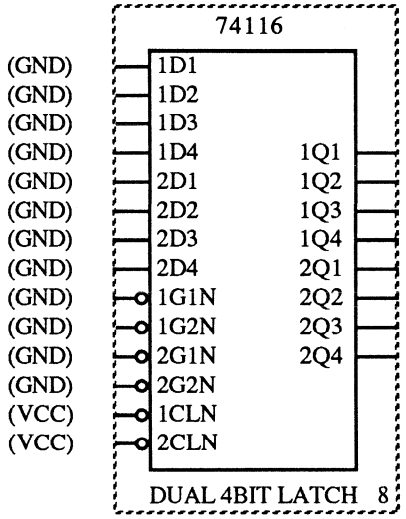
$Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}$ = level of the respective output before the last transition of the clock from low to high

* = shifting left requires connection of Q_B to A, Q_C to B, and Q_D to C. Serial data are entered at input D.

7499 Logic Schematic:



74116 (Latch)



Name: **74116** (Dual 4-Bit Latch With Clear)

Declaration: 74116(1D1,1D2,1D3,1D4,2D1,2D2,2D3, 2D4,1G1N,1G2N,2G1N,2G2N,1CLN,2CLN, 2Q4,2Q3,2Q2,2Q1,1Q4,1Q3,1Q2,1Q1)

EPLDs: All

Default Signal Levels: GND — 1D1, 1D2, 1D3, 1D4, 2D1, 2D2, 2D3, 2D4
VCC — 1CLN, 2CLN

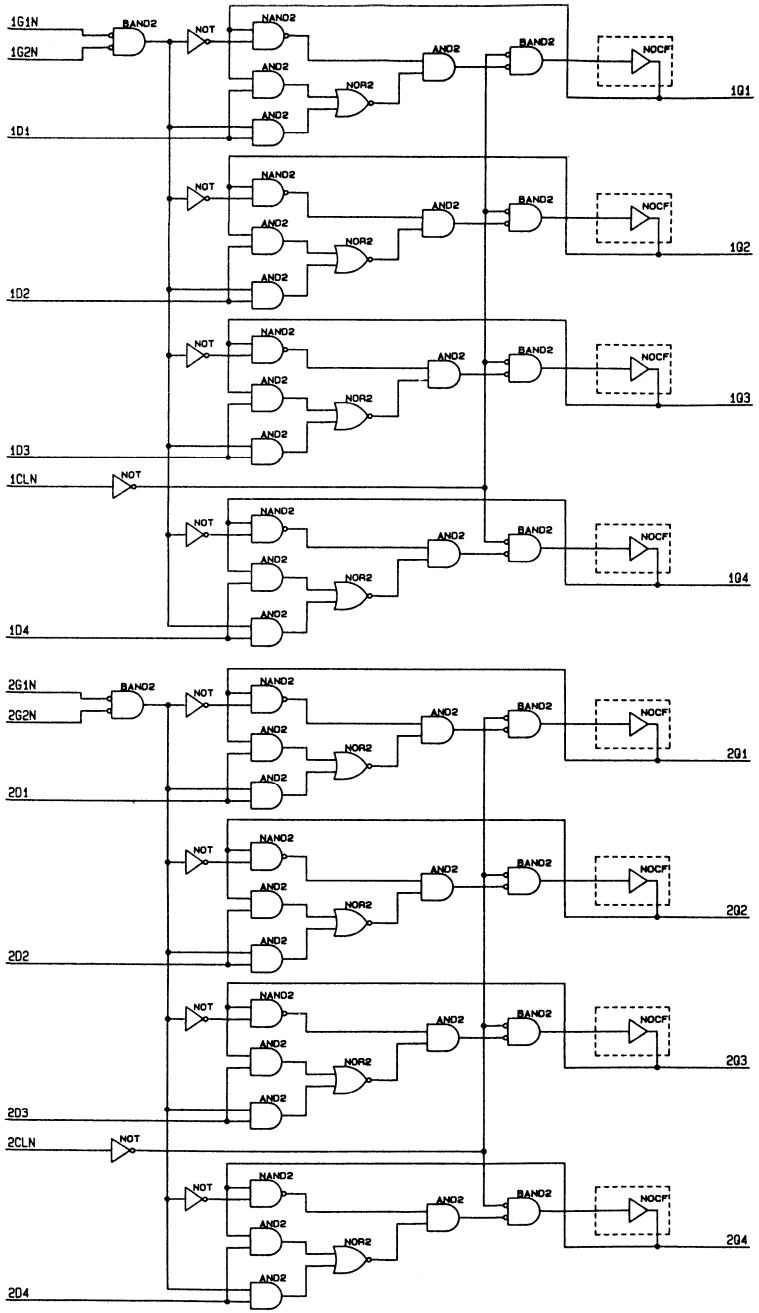
74116 Function Table:

74116 Function Table

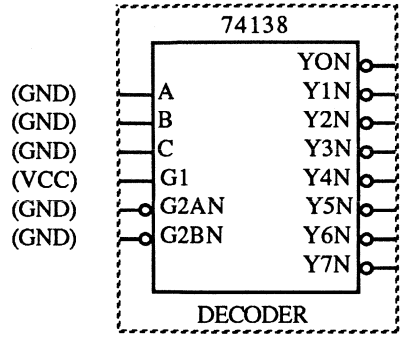
INPUTS				OUTPUT
CLEAR	ENABLE G1	ENABLE G2	D	Q
H	L	L	L	L
H	L	L	H	H
H	X	H	X	Qo
H	H	X	X	Qo
L	X	X	X	L

H = high level
L = low level
Qo = level of Q before these input conditions were established

74116 Logic Schematic:



74138 (Decoder)



Name: **74138** (3:8 Decoder)

Declaration: 74138(G1,G2AN,G2BN,A,B,C,D,Y7N,Y6N, Y5N,Y4N,Y3N,Y2N,Y1N,Y0N)

EPLDs: All

Default Signal Levels: GND — G2AN, G2BN, A, B, C
VCC — G1

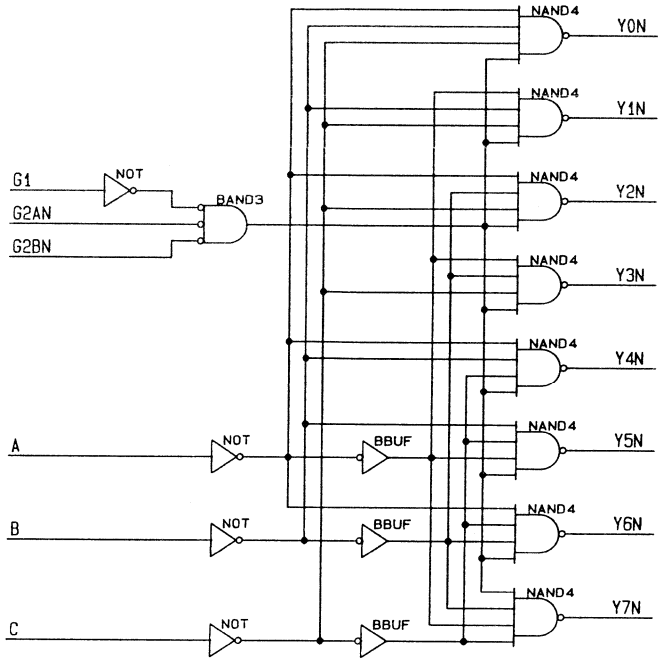
74138 Function Table:

74138 Function Table

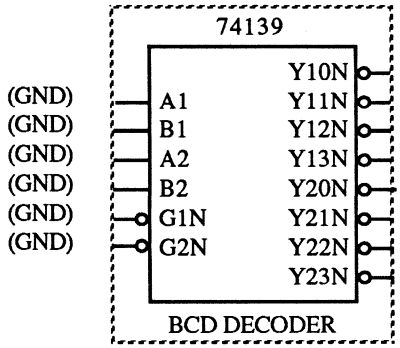
INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0N	Y1N	Y2N	Y3N	Y4N	Y5N	Y6N	Y7N
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2AN + G2BN
H = high level
L = low level
X = don't care

74138 Logic Schematic:



74139 (Decoder)



Name: **74139** (1:4 Decoder)

Declaration: 74139(G1N,G2N,A1,B1,A2,B2,Y23N,Y22N, Y21N,Y20N,Y13N,Y12N,Y11N,Y10N)

EPLDs: All

Default Signal Levels: GND — all input pins

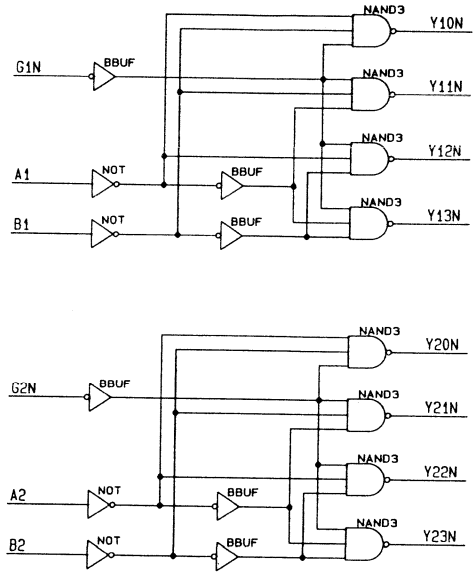
Function Table:

74139 Function Table

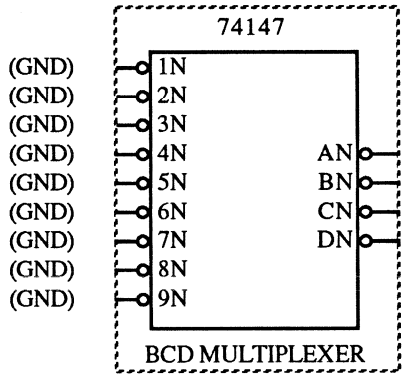
INPUTS			OUTPUTS			
ENABLE	SELECT					
GN	B	A	Y0N	Y1N	Y2N	Y3N
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level L = low level X = don't care

74139 Logic Schematic:



74147 (Multiplexer)



Name: **74147** (10-to-4 BCD Encoder)

Declaration: 74147(1N,2N,3N,4N,5N,6N,7N,8N,9N, DN,CN,BN,AN)

EPLDs: All

Default Signal Levels: GND — all input pins

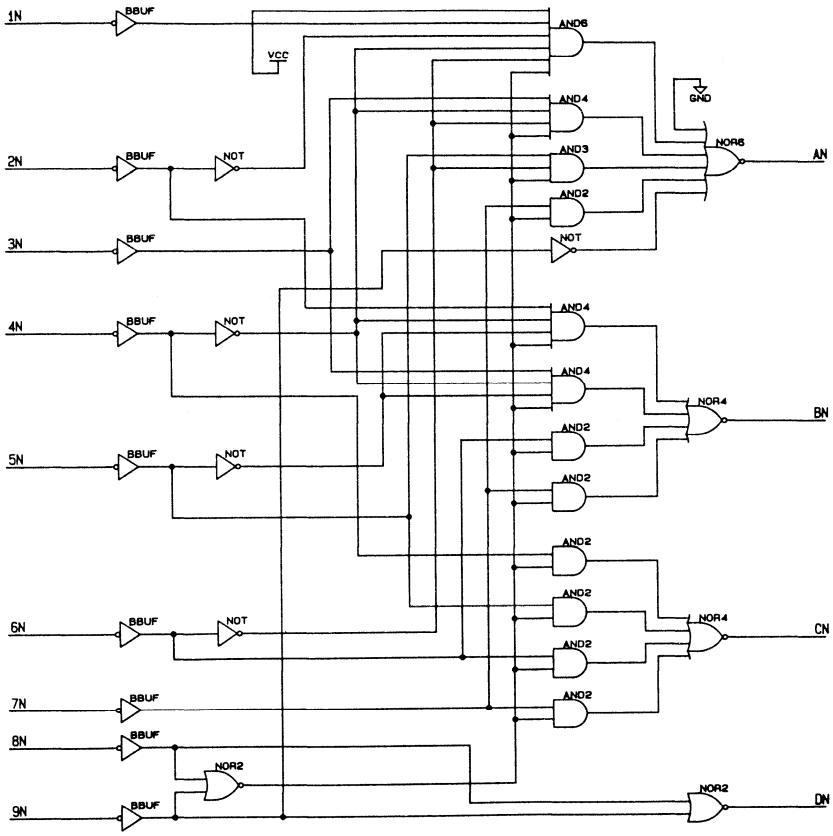
74147 Function Table:

74147 Function Table

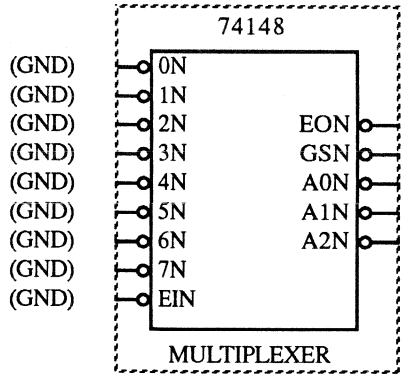
INPUTS									OUTPUTS			
1N	2N	3N	4N	5N	6N	7N	8N	9N	DN	CN	BN	AN
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = high level
L = low level
X = don't care

74147 Logic Schematic:



74148 (Multiplexer)



Name: **74148** (8-Line to 3-Line Octal Encoder)

Declaration: 74148(0N,1N,2N,3N,4N,5N,6N,7N,EIN, A2N,A1N,A0N,GSN,EON)

EPLDs: All

Default Signal Levels: GND — all input pins

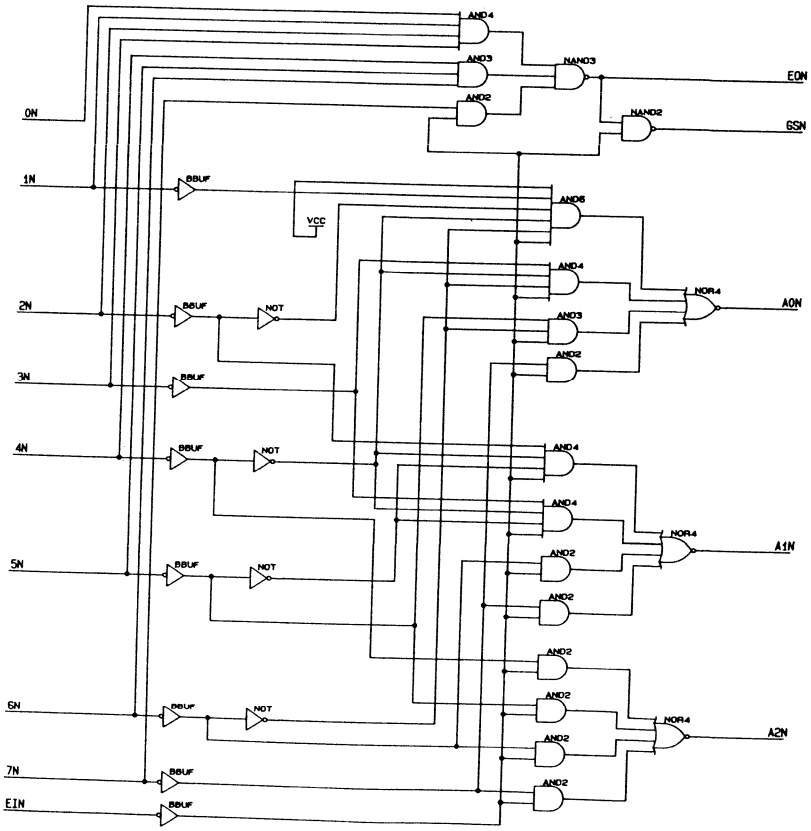
74148 Function Table:

74148 Function Table

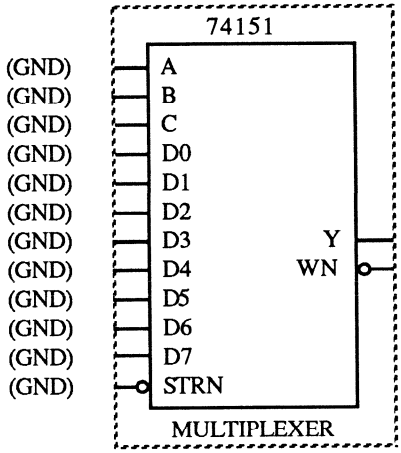
INPUTS									OUTPUTS				
E1N	0N	1N	2N	3N	4N	5N	6N	7N	A2N	A1N	A0N	GSN	EON
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high level L = low level X = don't care

74148 Logic Schematic:



74151 (Multiplexer)



Name: **74151** (8:1 Multiplexer)

Declaration: 74151(STRN,D0,D1,D2,D3,D4,D5,D6,D7,A, B,C,WN,Y)

EPLDs: All

Default Signal Levels: GND — all input pins

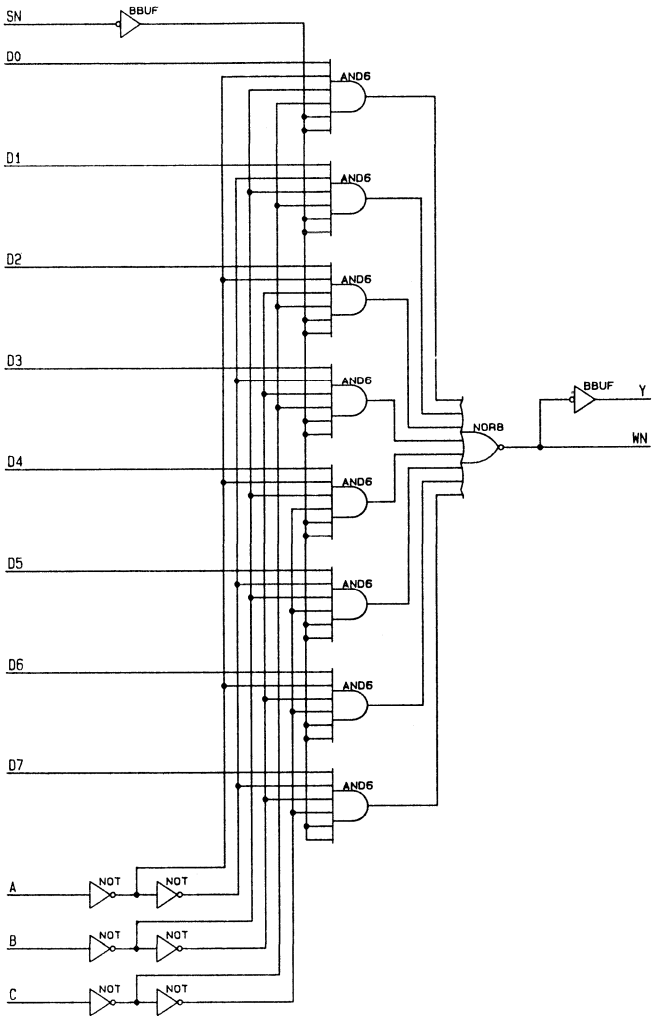
74151 Function Table:

74151 Function Table

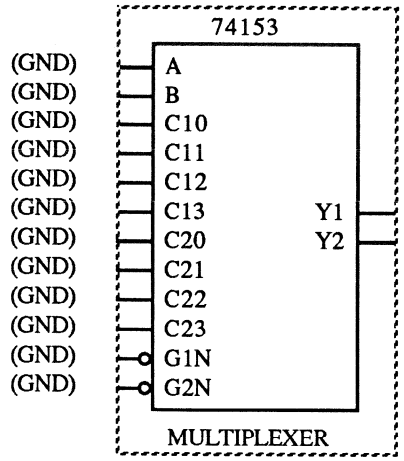
INPUTS				OUTPUTS	
SELECT			STROBE	Y	WN
C	B	A	SN		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level L = low level X = don't care
D0, D1, ... D7 = the level of the D input

74151 Logic Schematic:



74153 (Multiplexer)



Name: **74153** (Dual 4:1 Multiplexer)

Declaration: 74153(G1N,C10,C11,C12,C13,B,A,C20, C21,C22,C23,G2N,Y2,Y1)

EPLDs: All

Default Signal Levels: GND — all input pins

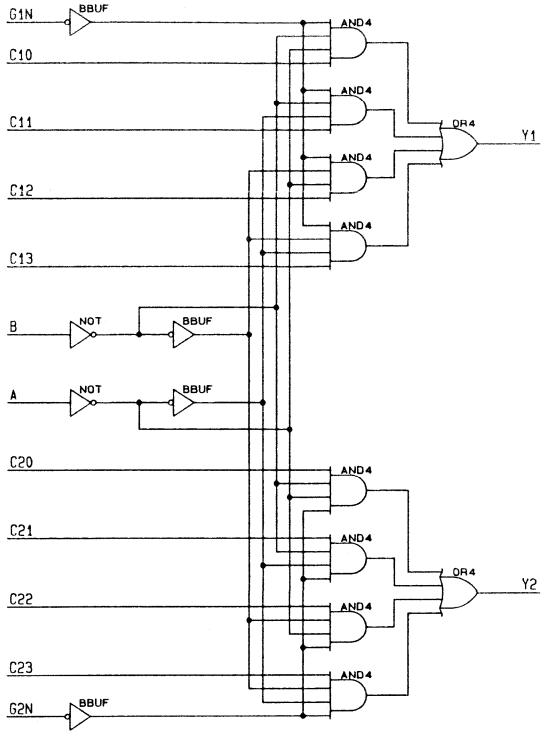
74153 Function Table:

74153 Function Table

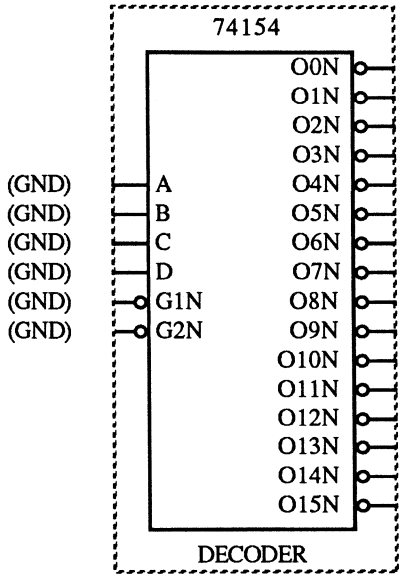
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	GN	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = high level L = low level X = don't care
Select inputs A and B are common to both sections.

74153 Logic Schematic:



74154 (Decoder)



Name: **74154** (4-to-16 Line Decoder)

Declaration: 74154(A,B,C,D,G1N,G2N,O15N,O14N, O13N,O12N,O11N,O10N,O9N,O8N,O7N, O6N,O5N,O4N,O3N,O2N,O1N,O0N)

EPLDs: EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

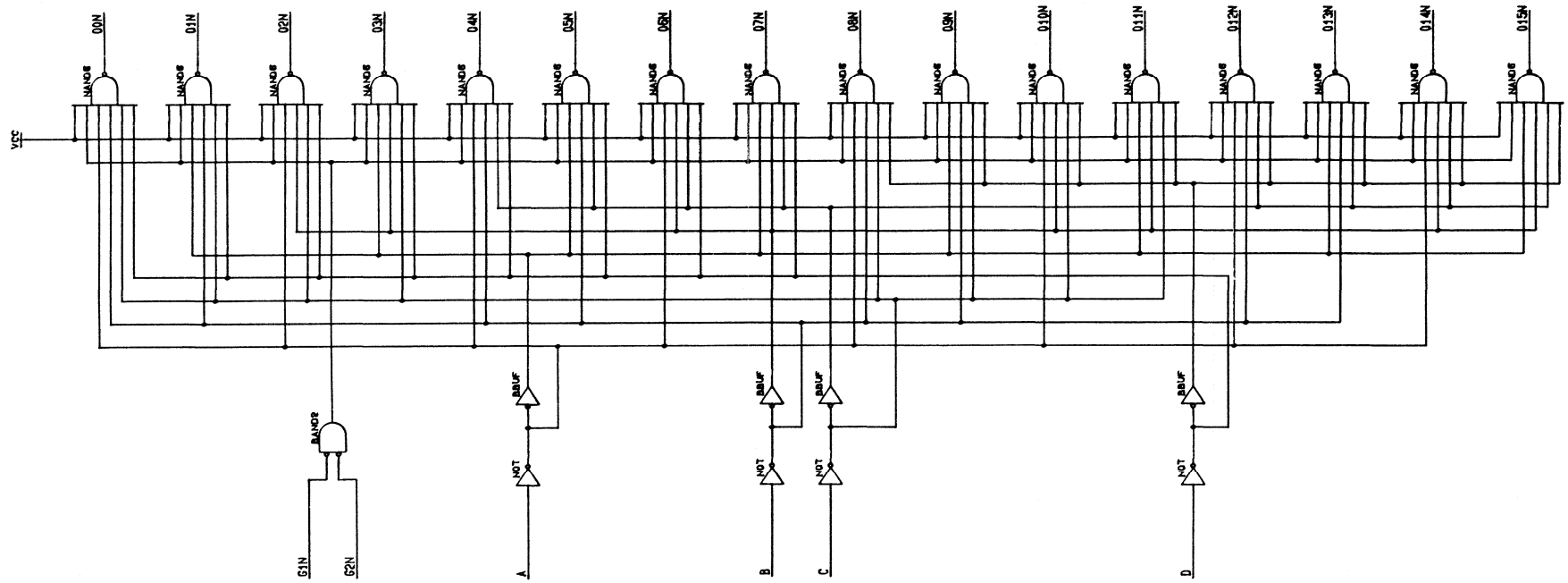
74154 Function Table:

74154 Function Table

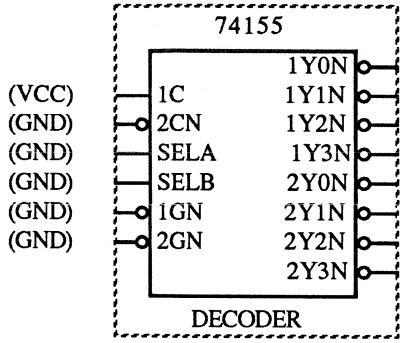
INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level
L = low level
X = don't care

74154 Logic Schematic:



74155 (Decoder)



Name: **74155** (1 to 4 Decoder)

Declaration: 74155(1C,2C,SELA,SELB,1G,2G,2Y3N, 2Y2N,2Y1N,2Y0N,1Y3N,1Y2N,1Y1N,1Y0N)

EPLDs: All

Default Signal Levels: GND — 2C, SELA, SELB, 1G, 2G
VCC — 1C

74155 Function Table:

74155 Function Table

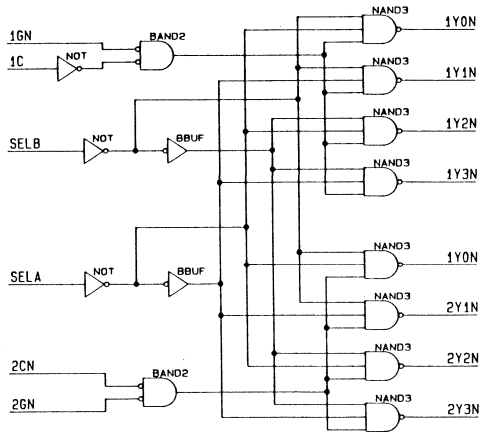
INPUTS				OUTPUTS			
SELECT B	SELECT A	STROBE 1GN	DATA 1C	1Y0N	1Y1N	1Y2N	1Y3N
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

H = high level L = low level X = don't care.

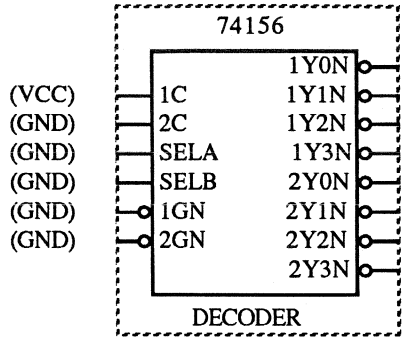
INPUTS				OUTPUTS			
SELECT B	SELECT A	STROBE 2GN	DATA 2C	2Y0N	2Y1N	2Y2N	2Y3N
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

H = high level L = low level X = don't care.

74155 Logic Schematic:



74156 (Decoder)



Name: **74156** (1 to 4 Decoder)

Declaration: 74156(1C,2C,SELA,SELB,1GN,2GN,2Y3N, 2Y2N,2Y1N,2Y0N,1Y3N,1Y2N,1Y1N,1Y0N)

EPLDs: All

Default Signal Levels: GND — 2C, SELA, SELB, 1GN, 2GN
VCC — 1C

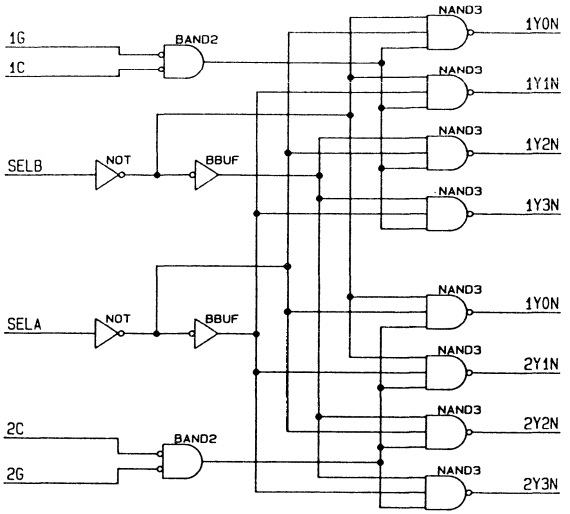
74156 Function Table:

74156 Function Table

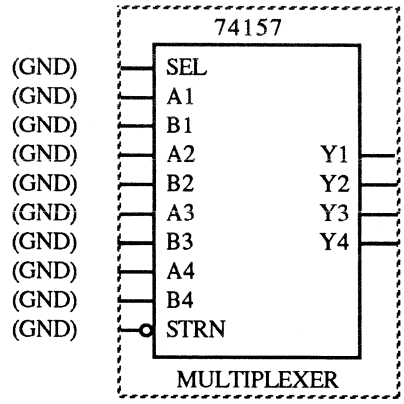
INPUTS				OUTPUTS							
SELECT C*	B	A	STROBE or DATA GN**	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	L	L	L
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H

H = high level L = low level X = don't care
*C = inputs 1C and 2C connected together
**GN = inputs 1GN and 2GN connected together

74156 Logic Schematic:



74157 (Multiplexer)



Name: **74157** (Quad 4:1 Multiplexer)

Declaration: 74157(A1,B1,A2,B2,A3,B3,A4,B4,STRN, SEL,Y4,Y3,Y2,Y1)

EPLDs: All

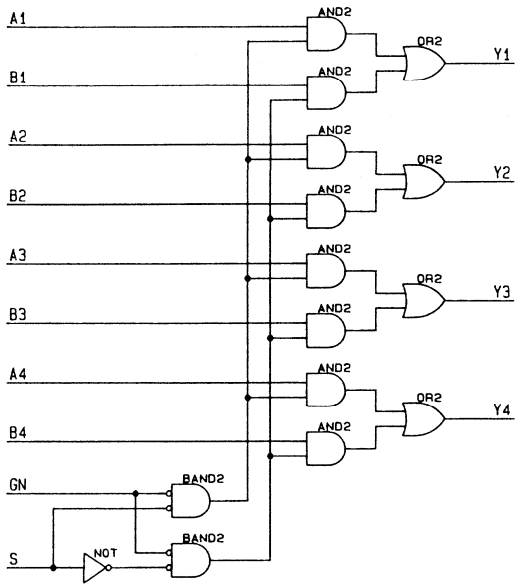
Default Signal Levels: GND — all input pins

Function Table:

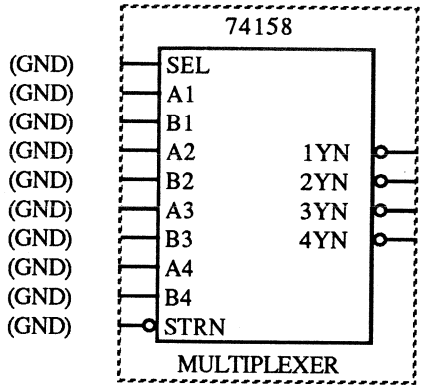
74157 Function Table

INPUTS				OUTPUT Y
STRN	SEL	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H = high level L = low level X = don't care				

74157 Logic Schematic:



74158 (Multiplexer)



Name: **74158** (Quad 2:1 Multiplexer)

Declaration: 74158(SEL,A1,B1,A2,B2,A3,B3,A4,B4, STRN,4YN,3YN,2YN,1YN)

EPLDs: All

Default Signal Levels: GND — all input pins

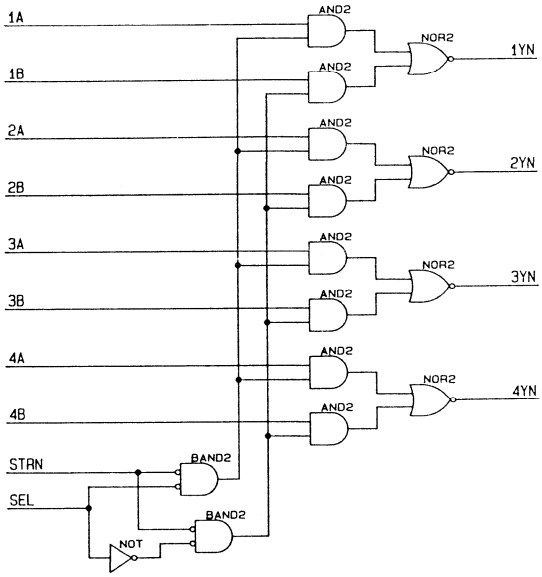
Function Table

74158 Function Table

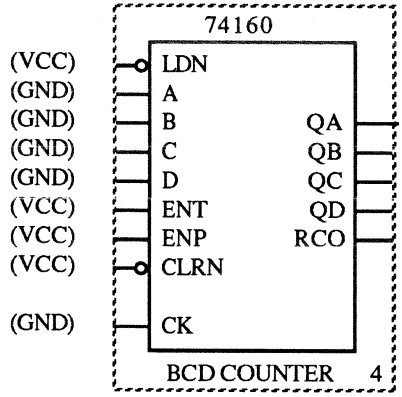
INPUTS				OUTPUT
STRN	SEL	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = high level L = low level
X = don't care

74158 Logic Schematic:



74160 (Counter)



Name: **74160** (4-Bit Decade Counter With Synchronous Load, Asynchronous Clear)

Declaration: 74160(CLRN,LDN,ENP,ENT,A,B,C,D,CK, QD,QC,QB,QA,RCO)

EPLDs: EP310, EP600, EP610 EP900, EP910 EP1210, EP1800, EPB1400

Default Signal Levels: GND — A, B, C, D, CK
VCC — LDN, ENT, ENP, CLRN

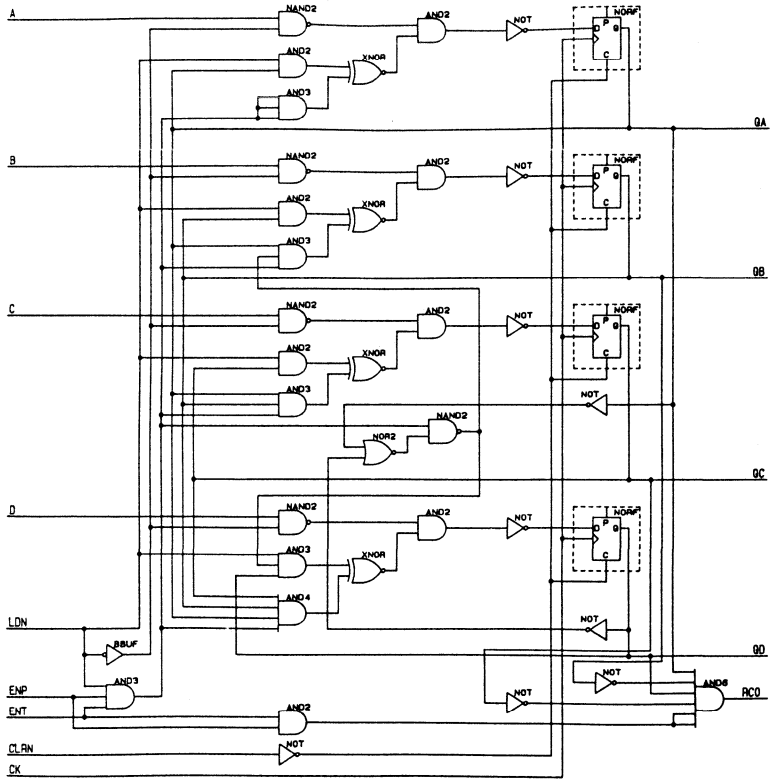
74160 Function Table:

74160 Function Table

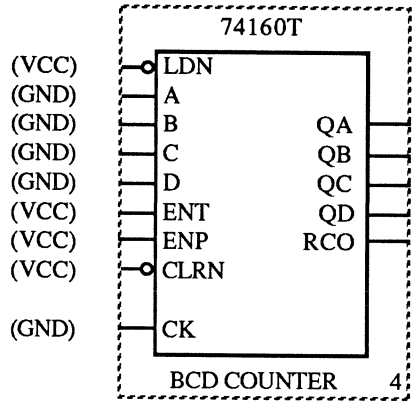
INPUTS									OUTPUTS				
CK	LDN	CLRN	ENP	ENT	D	C	B	A	Q_D	Q_C	Q_B	Q_A	RCO
X	X	L	X	X					L	L	L	L	L
⌐	L	H	X	X	d	c	b	a	d	c	b	a	L
⌐	H	H	X	L					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	L	X					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	H	H					L	L	L	L	L
⌐	H	H	H	H					L	L	L	H	L
⌐	H	H	H	H					L	L	H	L	L
⌐	H	H	H	H					L	L	H	H	L
⌐	H	H	H	H					L	H	L	L	L
⌐	H	H	H	H					L	H	L	H	L
⌐	H	H	H	H					L	H	H	L	L
⌐	H	H	H	H					L	H	H	H	L
⌐	H	H	H	H					H	L	L	L	L
⌐	H	H	H	H					H	L	L	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74160 Logic Schematic:



74160T (Counter)



Name: **74160T** (4-Bit Decade Counter With Clear)

Declaration: 74160T(LDN,A,B,C,D,ENT,ENP,CLRN,CK, RCO,QD,QC,QB,QA)

EPLDs: EP600, EP610 EP900, EP910 EP1800, EPB1400

Default Signal Levels: GND — A, B, C, D, CK
VCC — LDN, ENT, ENP, CLRN

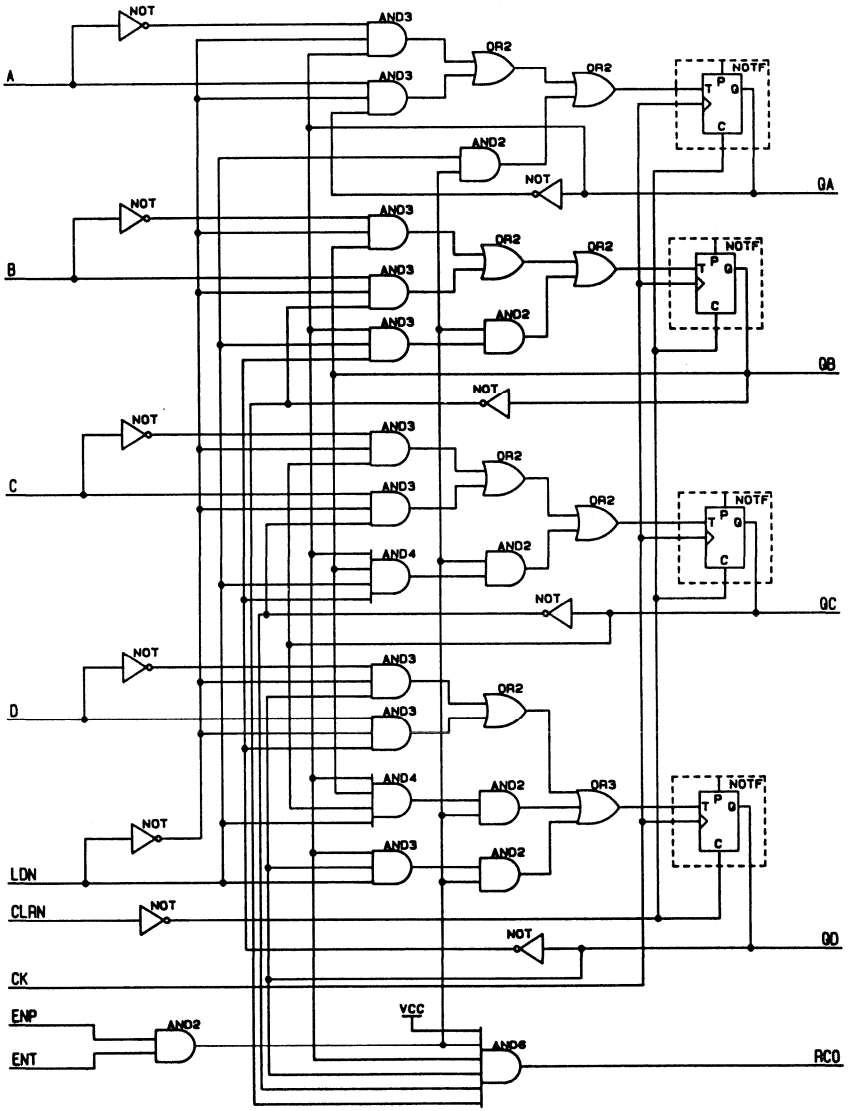
74160T Function Table:

74160T Function Table

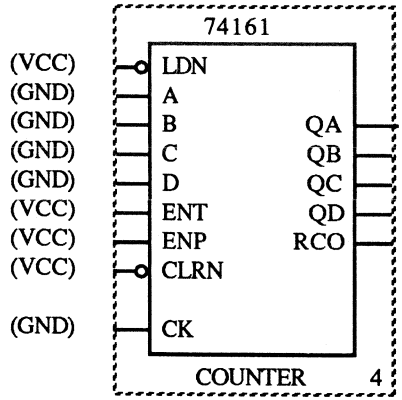
INPUTS									OUTPUTS				
CK	LDN	CLRN	ENP	ENT	D	C	B	A	Q_D	Q_C	Q_B	Q_A	RCO
X	X	L	X	X					L	L	L	L	L
⌐	L	H	X	X	d	c	b	a	d	c	b	a	L
⌐	H	H	X	L					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	L	X					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	H	H					L	L	L	L	L
⌐	H	H	H	H					L	L	L	H	L
⌐	H	H	H	H					L	L	H	L	L
⌐	H	H	H	H					L	L	H	H	L
⌐	H	H	H	H					L	H	L	L	L
⌐	H	H	H	H					L	H	L	H	L
⌐	H	H	H	H					L	H	H	L	L
⌐	H	H	H	H					L	H	H	H	L
⌐	H	H	H	H					H	L	L	L	L
⌐	H	H	H	H					H	L	L	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74160T Logic Schematic:



74161 (Counter)



Name: **74161** (4-Bit Binary Up Counter - Synchronous Load, Asynchronous Clear)

Declaration: 74161(CLRN,LDN,ENP,ENT,A,B,C,D,CK, QD,QC,QB,QA,RCO)

EPLDs: EP310, EP600, EP610 EP900, EP910 EP1210, EP1800, EPB1400

Default Signal Levels: GND — A, B, C, D, CK
VCC — LDN, ENT, ENP, CLRN

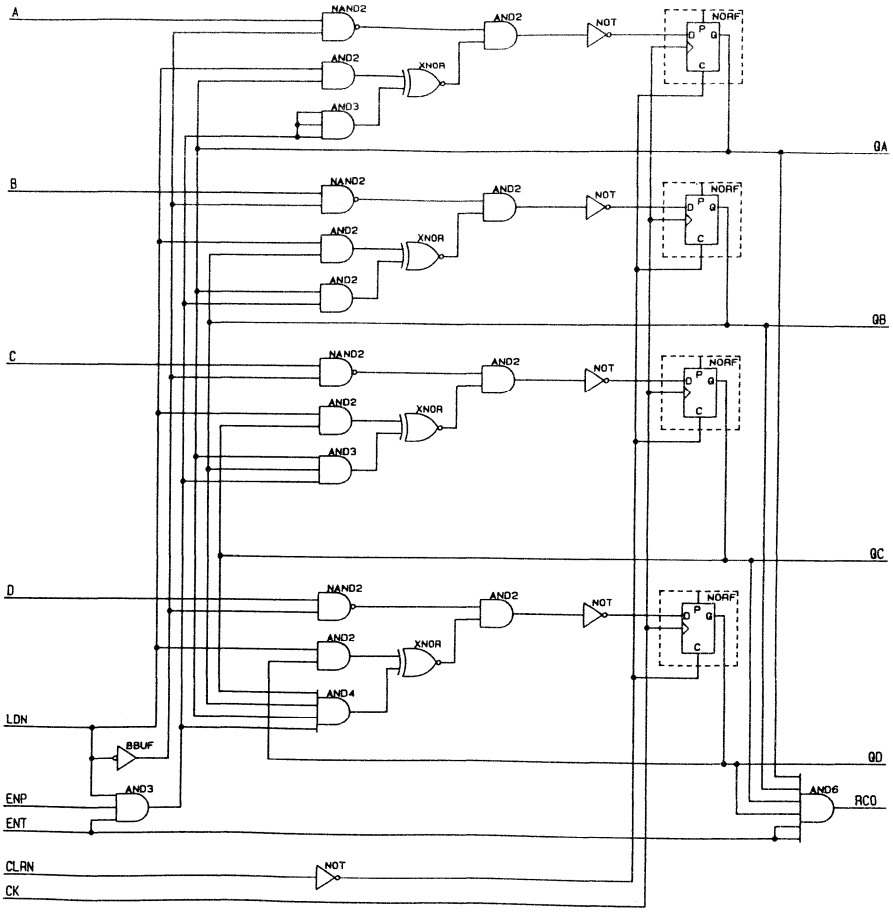
74161 Function Table:

74161 Function Table

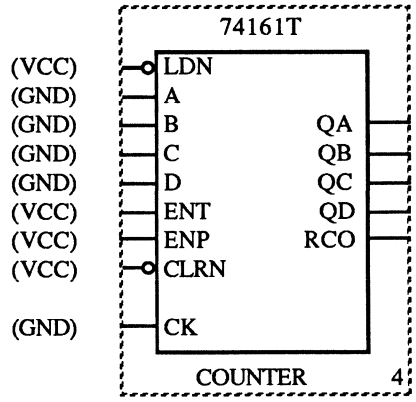
INPUTS									OUTPUTS				
CK	LDN	CLRN	ENP	ENT	D	C	B	A	Q_D	Q_C	Q_B	Q_A	RCO
X	X	L	X	X					L	L	L	L	L
⌐	L	H	X	X	d	c	b	a	d	c	b	a	L
⌐	H	H	X	H					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	L	L					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	H	H					L	L	L	L	L
⌐	H	H	H	H					L	L	L	H	L
⌐	H	H	H	H					L	L	H	L	L
⌐	H	H	H	H					L	L	H	H	L
⌐	H	H	H	H					L	H	L	L	L
⌐	H	H	H	H					L	H	L	H	L
⌐	H	H	H	H					L	H	H	L	L
⌐	H	H	H	H					L	H	H	H	L
⌐	H	H	H	H					H	L	L	L	L
⌐	H	H	H	H					H	L	L	H	L
⌐	H	H	H	H					H	L	H	L	L
⌐	H	H	H	H					H	L	H	H	L
⌐	H	H	H	H					H	H	L	L	L
⌐	H	H	H	H					H	H	L	H	L
⌐	H	H	H	H					H	H	H	L	L
X	H	H	H	H					H	H	H	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74161 Logic Schematic:



74161T (Counter)



Name: **74161T** (4-Bit Binary Counter With Clear)

Declaration: 74161T(LDN,A,B,C,D,ENT,ENP,CLRN,CK, RCO,QD,QC,QB,QA)

EPLDs: EP600, EP610 EP900, EP910 EP1800, EPB1400

Default Signal Levels: GND — A, B, C, D, CK
VCC — LDN, ENT, ENP, CLRN

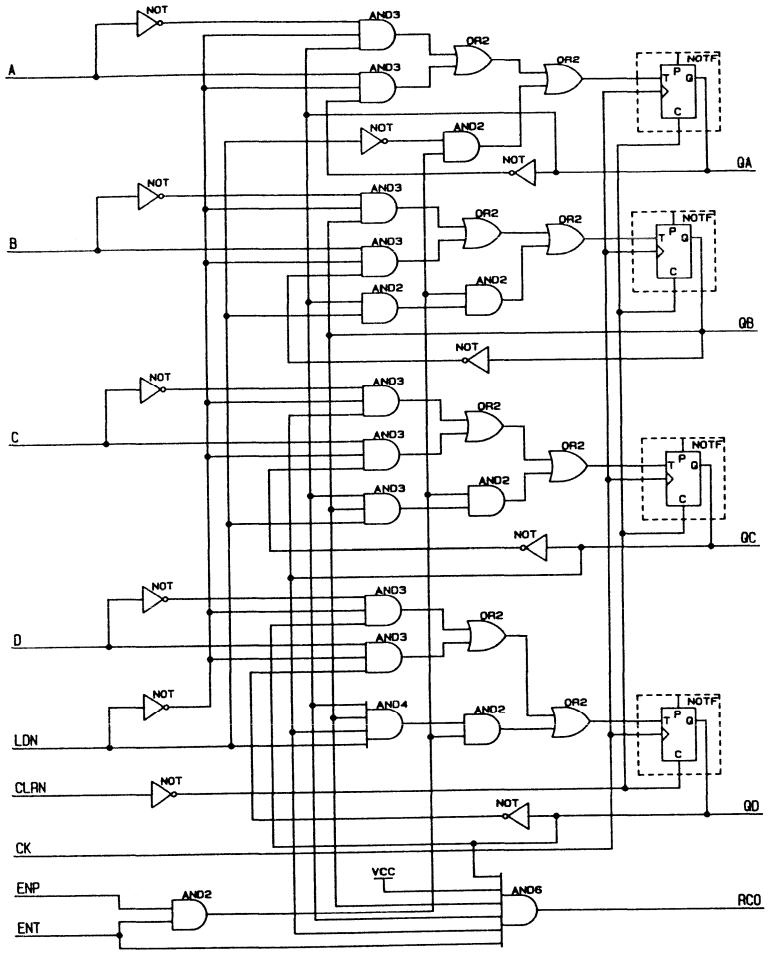
74161T Function Table:

74161T Function Table

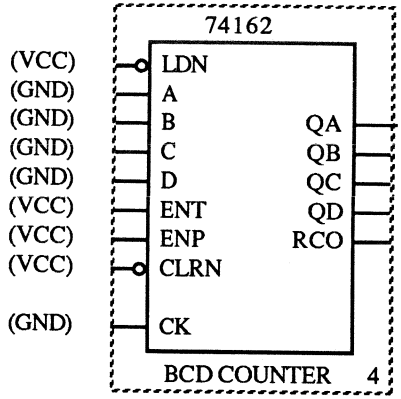
INPUTS									OUTPUTS				
CK	LDN	CLRN	ENP	ENT	D	C	B	A	Q_D	Q_C	Q_B	Q_A	RCO
X	X	L	X	X					L	L	L	L	L
⌐	L	H	X	X	d	c	b	a	d	c	b	a	L
⌐	H	H	X	H					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	L	L					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	H	H					L	L	L	L	L
⌐	H	H	H	H					L	L	L	H	L
⌐	H	H	H	H					L	L	H	L	L
⌐	H	H	H	H					L	L	H	H	L
⌐	H	H	H	H					L	H	L	L	L
⌐	H	H	H	H					L	H	L	H	L
⌐	H	H	H	H					L	H	H	L	L
⌐	H	H	H	H					L	H	H	H	L
⌐	H	H	H	H					H	L	L	L	L
⌐	H	H	H	H					H	L	L	H	L
⌐	H	H	H	H					H	L	H	L	L
⌐	H	H	H	H					H	L	H	H	L
⌐	H	H	H	H					H	H	L	L	L
⌐	H	H	H	H					H	H	L	H	L
⌐	H	H	H	H					H	H	H	L	L
X	H	H	H	H					H	H	H	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74161T Logic Schematic:



74162 (Counter)



Name: **74162** (4-Bit Up Decade Counter With Synchronous Load and Clear)

Declaration: 74162(CLRN,LDN,ENP,ENT,A,B,C,D,CK, QD,QC,QB,QA,RCO)

EPLDs: All

Default Signal Levels: GND — A, B, C, D, CK
VCC — LDN, ENT, ENP, CLRN

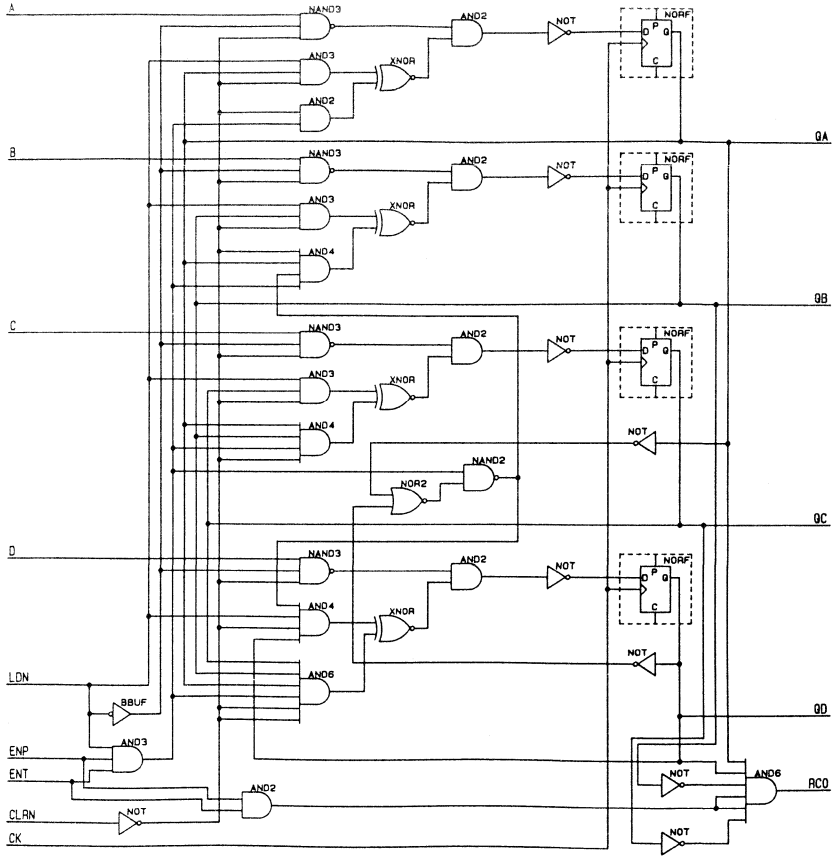
74162 Function Table:

74162 Function Table

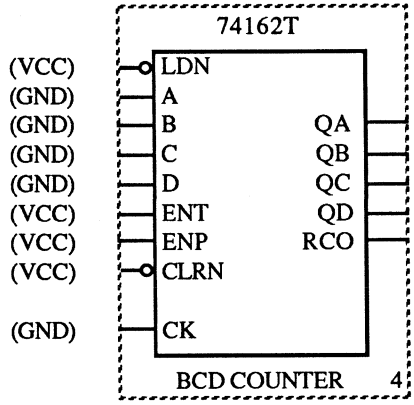
INPUTS									OUTPUTS				
CK	LDN	CLRN	ENP	ENT	D	C	B	A	Q_D	Q_C	Q_B	Q_A	RCO
⌐	X	L	X	X					L	L	L	L	L
⌐	L	H	X	X	d	c	b	a	d	c	b	a	L
⌐	H	H	X	L					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	L	X					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	H	H					L	L	L	L	L
⌐	H	H	H	H					L	L	L	H	L
⌐	H	H	H	H					L	L	H	L	L
⌐	H	H	H	H					L	L	H	H	L
⌐	H	H	H	H					L	H	L	L	L
⌐	H	H	H	H					L	H	L	H	L
⌐	H	H	H	H					L	H	H	L	L
⌐	H	H	H	H					L	H	H	H	L
⌐	H	H	H	H					H	L	L	L	L
X	H	H	H	H					H	L	L	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74162 Logic Schematic:



74162T (Counter)



Name: **74162T** (4-Bit DecadeCounter With Synchronous Clear)

Declaration: 74162T(LDN,A,B,C,D,ENT,ENP,CLRN,CK, RCO,QD,QC,QB,QA)

EPLDs: EP600, EP610 EP900, EP910 EP1800, EPB1400

Default Signal Levels: GND — A, B, C, D, CK
VCC — LDN, ENT, ENP, CLRN

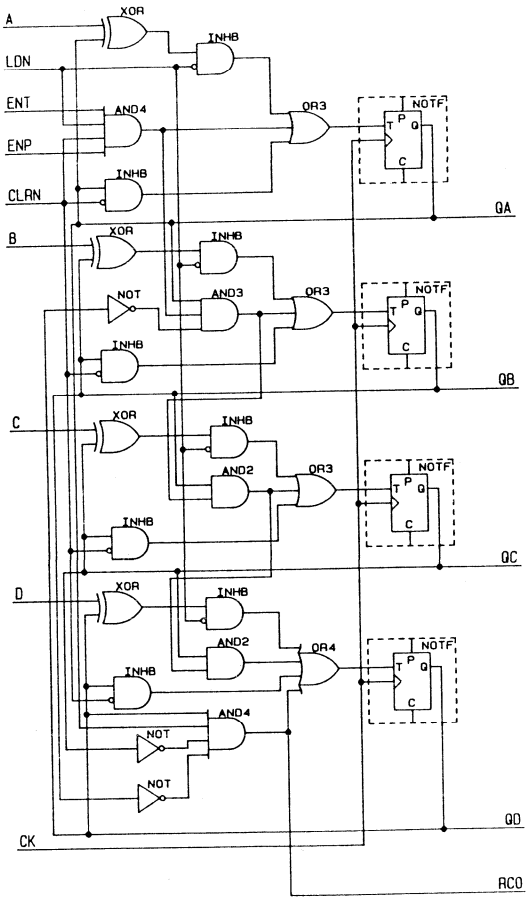
74162T Function Table:

74162T Function Table

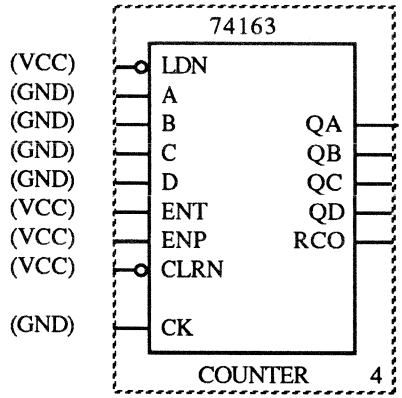
INPUTS									OUTPUTS				
CK	LDN	CLRN	ENP	ENT	D	C	B	A	Q_D	Q_C	Q_B	Q_A	RCO
⌐	X	L	X	X					L	L	L	L	L
⌐	L	H	X	X	d	c	b	a	d	c	b	a	L
⌐	H	H	X	L					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	L	X					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	H	H					L	L	L	L	L
⌐	H	H	H	H					L	L	L	H	L
⌐	H	H	H	H					L	L	H	L	L
⌐	H	H	H	H					L	L	H	H	L
⌐	H	H	H	H					L	H	L	L	L
⌐	H	H	H	H					L	H	L	H	L
⌐	H	H	H	H					L	H	H	L	L
⌐	H	H	H	H					L	H	H	H	L
⌐	H	H	H	H					H	L	L	L	L
X	H	H	H	H					H	L	L	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74162T Logic Schematic:



74163 (Counter)



Name: **74163** (4-Bit Up Binary Counter With Synchronous Load and Clear)

Declaration: 74163(CLRN,LDN,ENP,ENT,A,B,C,D,CK, QD,QC,QB,QA,RCO)

EPLDs: All

Default Signal Levels: GND — A, B, C, D, CK
VCC — LDN, ENT, ENP, CLRN

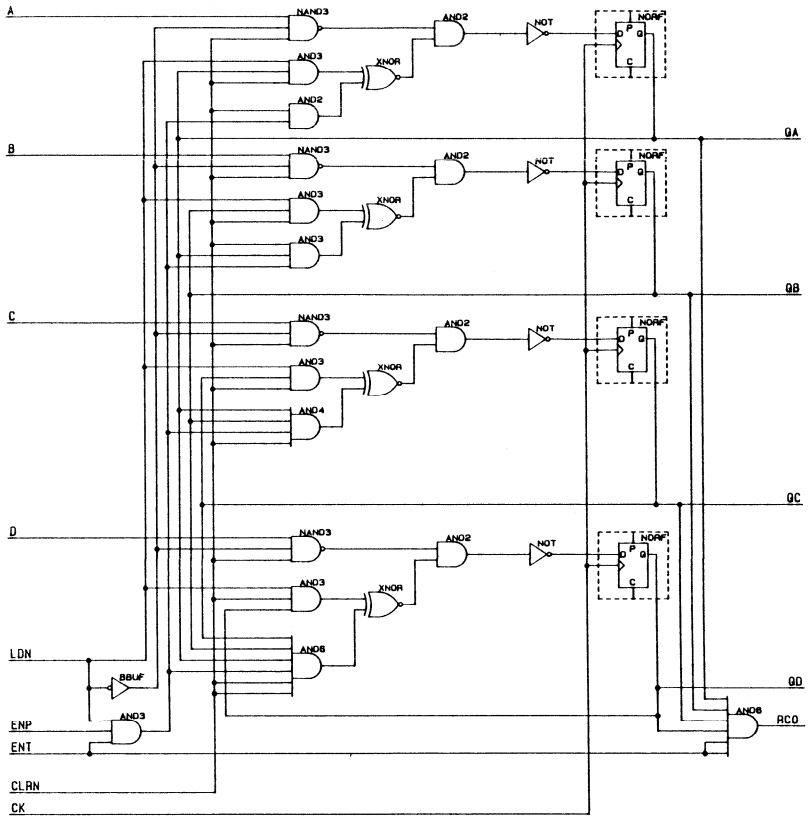
74163 Function Table:

74163 Function Table

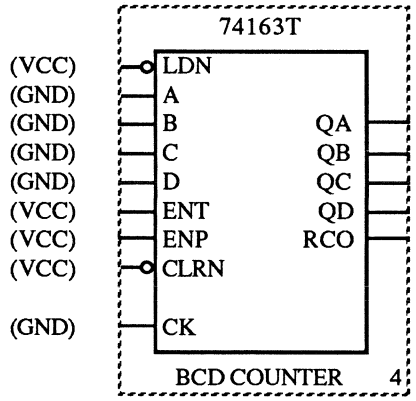
INPUTS									OUTPUTS				
CK	LDN	CLRN	ENP	ENT	D	C	B	A	Q_D	Q_C	Q_B	Q_A	RCO
⌐	X	L	X	X					L	L	L	L	L
⌐	L	H	X	X	d	c	b	a	d	c	b	a	L
⌐	H	H	L	H					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	H	L					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	H	H					L	L	L	L	L
⌐	H	H	H	H					L	L	L	H	L
⌐	H	H	H	H					L	L	H	L	L
⌐	H	H	H	H					L	L	H	H	L
⌐	H	H	H	H					L	H	L	L	L
⌐	H	H	H	H					L	H	L	H	L
⌐	H	H	H	H					L	H	H	L	L
⌐	H	H	H	H					L	H	H	H	L
⌐	H	H	H	H					H	L	L	L	L
⌐	H	H	H	H					H	L	L	H	L
⌐	H	H	H	H					H	L	H	L	L
⌐	H	H	H	H					H	L	H	H	L
⌐	H	H	H	H					H	H	L	L	L
⌐	H	H	H	H					H	H	L	H	L
⌐	H	H	H	H					H	H	H	L	L
X	H	H	H	H					H	H	H	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74163 Logic Schematic:



74163T (Counter)



Name: **74163T** (4-Bit Binary Counter With Synchronous Clear)

Declaration: 74163T(LDN,A,B,C,D,ENT,ENP,CLRN,CK, RCO,QD,QC,QB,QA)

EPLDs: EP600, EP610 EP900, EP910 EP1800, EPB1400

Default Signal Levels: GND — A, B, C, D, CK
VCC — LDN, ENT, ENP, CLRN

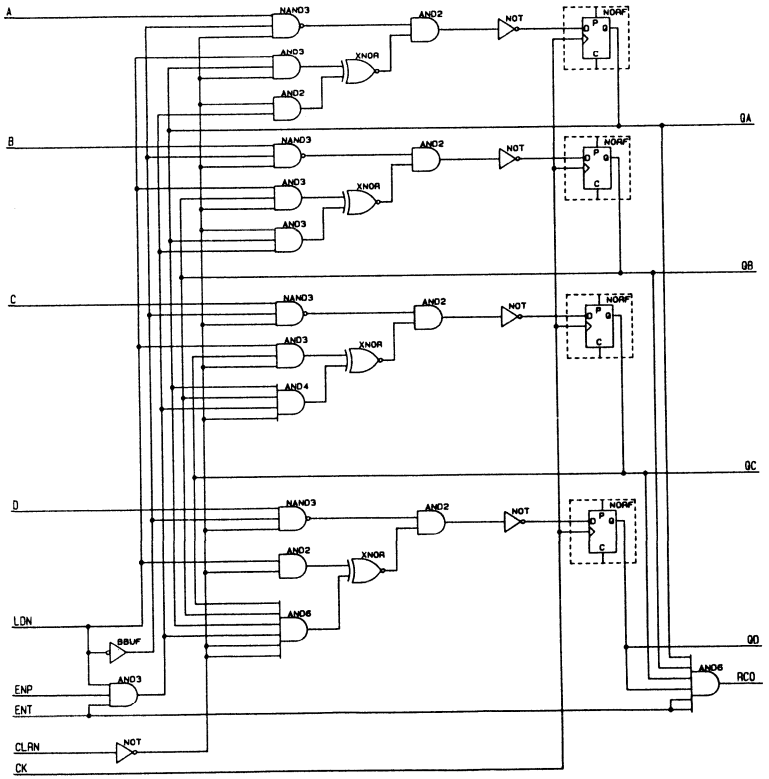
74163T Function Table:

74163T Function Table

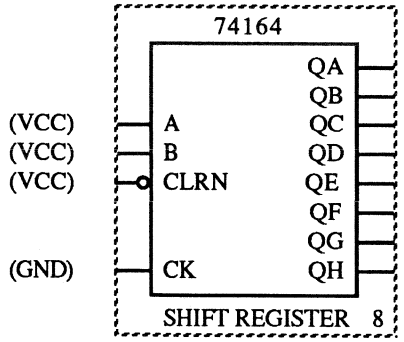
INPUTS									OUTPUTS				
CK	LDN	CLRN	ENP	ENT	D	C	B	A	Q_D	Q_C	Q_B	Q_A	RCO
⌐	X	L	X	X					L	L	L	L	L
⌐	L	H	X	X	d	c	b	a	d	c	b	a	L
⌐	H	H	L	H					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	H	L					Q_D	Q_C	Q_B	Q_A	L
⌐	H	H	H	H					L	L	L	L	L
⌐	H	H	H	H					L	L	L	H	L
⌐	H	H	H	H					L	L	H	L	L
⌐	H	H	H	H					L	L	H	H	L
⌐	H	H	H	H					L	H	L	L	L
⌐	H	H	H	H					L	H	L	H	L
⌐	H	H	H	H					L	H	H	L	L
⌐	H	H	H	H					L	H	H	H	L
⌐	H	H	H	H					H	L	L	L	L
⌐	H	H	H	H					H	L	L	H	L
⌐	H	H	H	H					H	L	H	L	L
⌐	H	H	H	H					H	L	H	H	L
⌐	H	H	H	H					H	H	L	L	L
⌐	H	H	H	H					H	H	L	H	L
⌐	H	H	H	H					H	H	H	L	L
X	H	H	H	H					H	H	H	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74163T Logic Schematic:



74164 (Shift Register)



Name: **74164** (Serial-In Parallel-Out Shift Register)

Declaration: 74164(A,B,CLRN,CK,QH,QG,QF,QE,QD, QC,QB,QA)

EPLDs: EP310, EP600, EP610 EP900, EP910 EP1210, EP1800, EPB1400

Default Signal Levels: GND — CK
VCC — A, B, CLRN

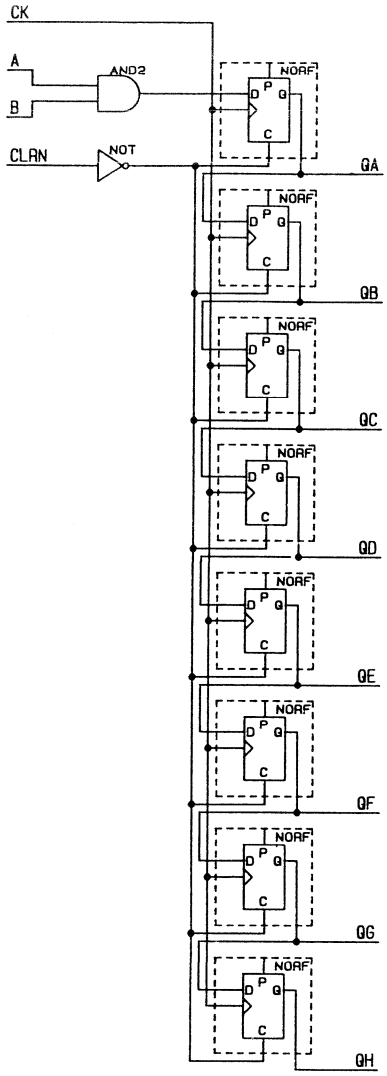
74164 Function Table:

74164 Function Table

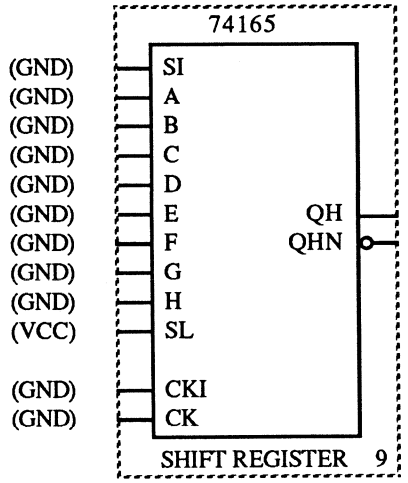
INPUTS				OUTPUTS		
CK	CLRN	A	B	Q_A	Q_B ...	Q_H
X	L	X	X	L	L	L
L	H	X	X	Q_{A0}	Q_{B0}	Q_{H0}
⌐	H	H	H	H	Q_{An}	Q_{Gn}
⌐	H	L	X	L	Q_{An}	Q_{Gn}
⌐	H	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
Q_{AO}, Q_{B0}, Q_{HO} = level of Q_A, Q_B, Q_H before the indicated steady-state input conditions were established
Q_{An}, Q_{Gn} = level of Q_A or Q_G before the most recent ⌐ transition of the clock; indicates a one-bit shift.

74164 Logic Schematic:



74165 (Shift Register)



Name: **74165** (Parallel Load 8-Bit Shift Register)

Declaration: 74165(SI,A,B,C,D,E,F,G,H,SL,CKI,CK, QHN,QH)

EPLDs: EP600, EP610 EP900, EP910 EP1210, EP1800, EPB1400

Default Signal Levels: GND — SI, A, B, C, D, E, F, G, H, CKI, CK
VCC — SL

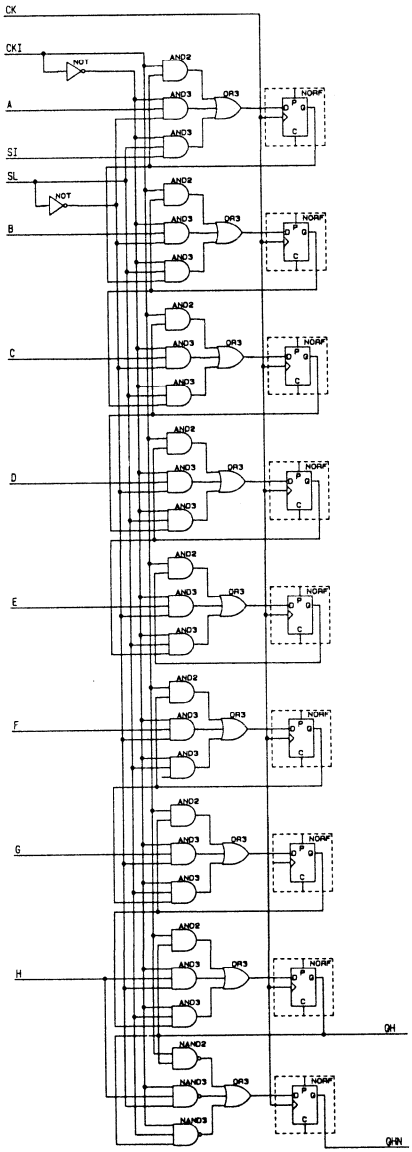
74165 Function Table:

74165 Function Table

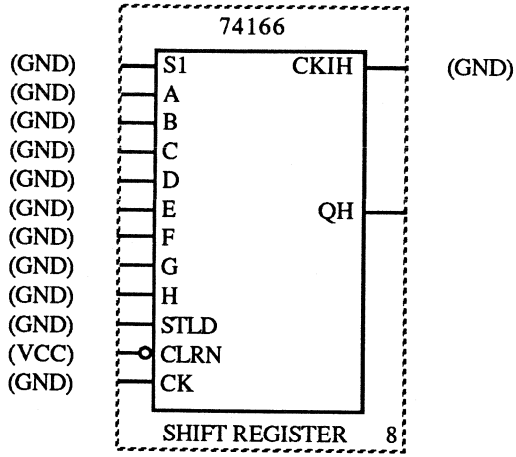
INPUTS					INTERNAL OUTPUTS		OUTPUT
CK	CKI	SL	SI	PARALLEL			
				A ... H	Q_A	Q_B	Q_H
⌐	L	L	X	a ... h	a	b	h
L	L	H	X	X	Q_{A0}	Q_{B0}	Q_{H0}
⌐	L	H	H	X	H	Q_{An}	Q_{Gn}
⌐	L	H	L	X	L	Q_{An}	Q_{Gn}
X	H	H	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = high level (steady state)
L = low level (steady state)
⌐ = transition from low to high level
X = don't care (any input, including transitions)
a ... h = level of steady-state inputs at inputs A through H
Q_0 = level of Q before the indicated steady-state input conditions were established
Q_n = level of Q before the most recent active transition indicated by ⌐

74165 Logic Schematic:



74166 (Shift Register)



Name: **74166** (8-Bit Shift Register With Clock Inhibit)

Declaration: 74166(S1,A,B,C,D,E,F,G,H,STLD,CLRN, CKIH,CK,QH)

EPLDs: All

Default Signal Levels: GND — S1,A, B, C, D, E, F, G, H, STLD, CK, CKIH
VCC — CLRN

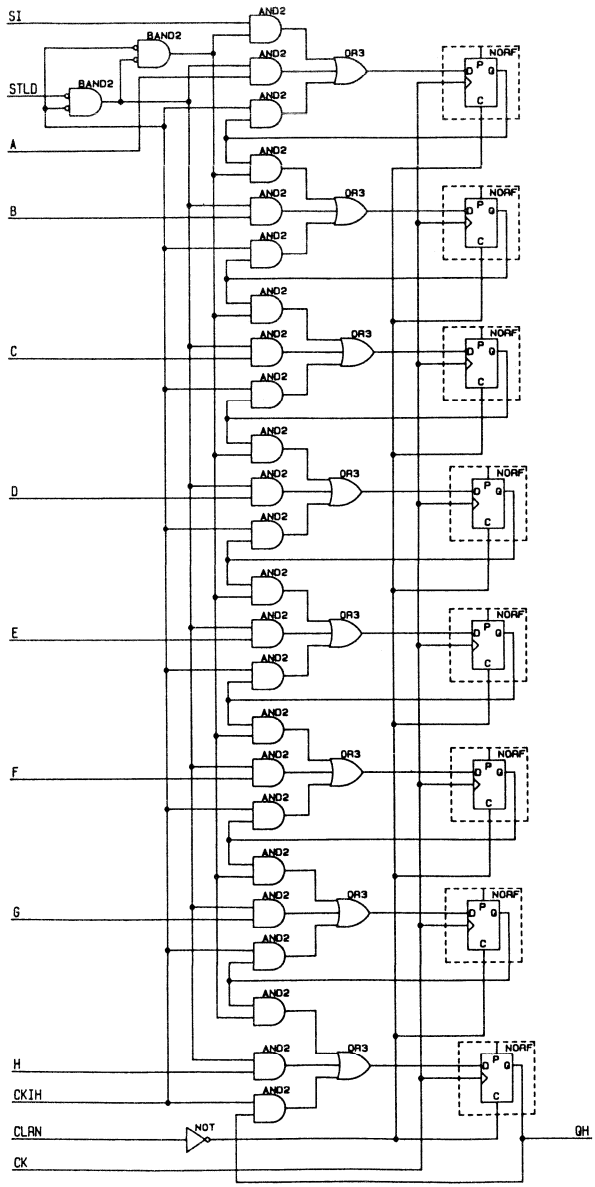
74166 Function Table:

74166 Function Table

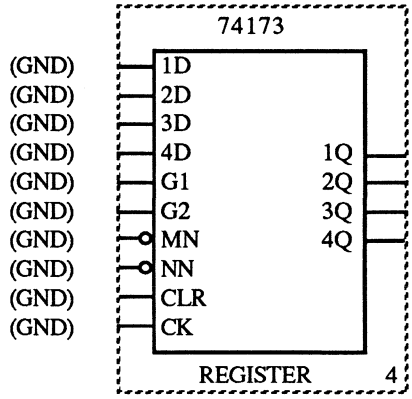
INPUTS						OUTPUT		
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SI	PARALLEL A ... H	INTERNAL Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	⌐	X	a ... h	a	b	h
H	H	L	⌐	H	X	H	Q_{An}	Q_{Gn}
H	H	L	⌐	L	X	L	Q_{An}	Q_{Gn}
H	X	H	⌐	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = high level (steady state)
L = low level (steady state)
⌐ = transition from low to high level
X = don't care (any input, including transitions)
a ... h = level of steady-state inputs at inputs A through H
Q_0 = level of Q before the indicated steady-state input conditions were established
Q_n = level of Q before the most recent active transition indicated by ⌐

74166 Logic Schematic:



74173 (Register)



Name: **74173** (4-Bit D-Type Register)

Declaration: 74173(1D,2D,3D,4D,G1,G2,MN,NN,CLR, CK,4Q,3Q,2Q,1Q)

EPLDs: EP310, EP600, EP610 EP900, EP910 EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

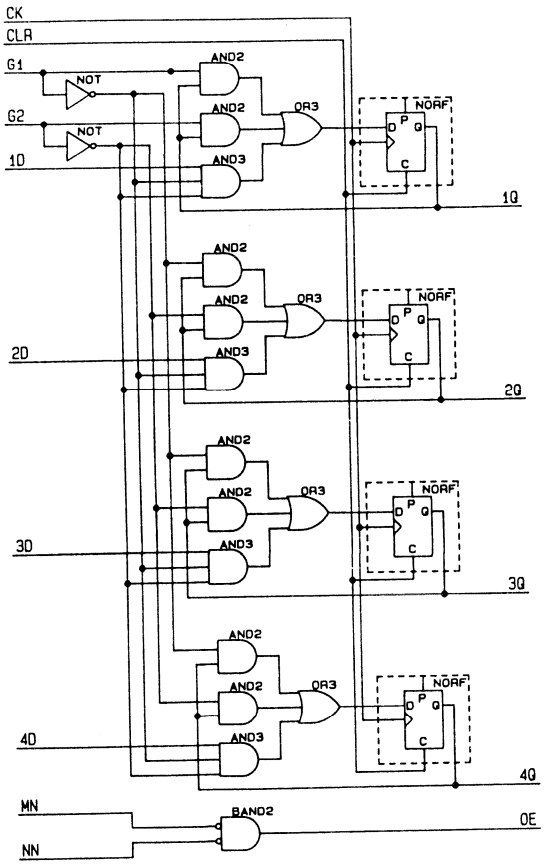
74173 Function Table:

74173 Function Table

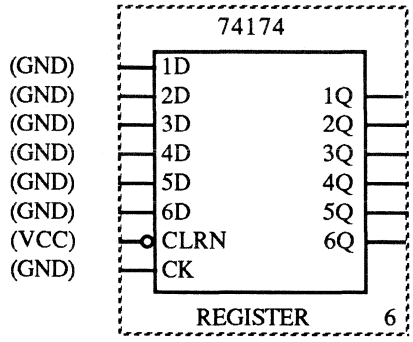
INPUTS					OUTPUT
CLEAR	CLOCK	DATA ENABLE G1	DATA ENABLE G2	D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	⌐	H	X	X	Q_0
L	⌐	X	H	X	Q_0
L	⌐	L	L	L	L
L	⌐	L	L	H	H

H = high level (steady state)
L = low level (steady state)
⌐ = transition from low to high level
X = don't care (any input, including transitions)
Q_0 = level of Q before the indicated steady-state input conditions were established
When either M or N is high, the output is low; however, sequential operation of the flipflop is not affected.

74173 Logic Schematic:



74174 (Register)



Name: **74174** (Hex D-Type Flipflop With Common Clear)

Declaration: 74174(1D,2D,3D,4D,5D,6D,CLRN,CK,6Q, 5Q,4Q,3Q,2Q,1Q)

EPLDs: EP310, EP600, EP610 EP900, EP910 EP1210, EP1800, EPB1400

Default Signal Levels: GND — 1D, 2D, 3D, 4D, 5D, 6D, CK
VCC — CLRN

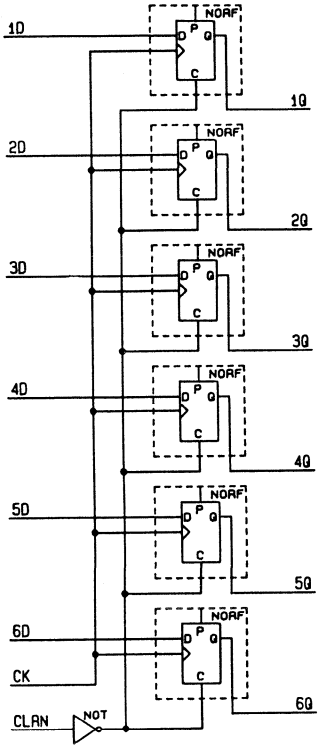
Function Table:

74174 Function Table

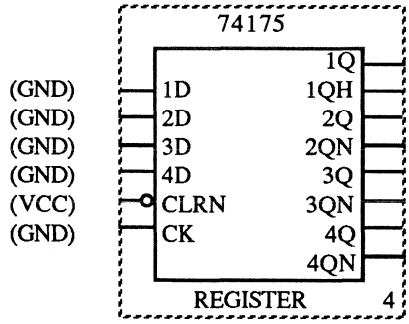
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	⌐	L	L
H	⌐	H	H
H	L	X	Q0

H = high level (steady state)
L = low level (steady state)
⌐ = transition from low to high
X = don't care
Q0 = level of Q before the indicated steady-state input conditions were established

74174 Logic Schematic:



74175 (Register)



Name: **74175** (Quad D-Type Flipflop With Common Clock and Clear)

Declaration: 74175(1D,2D,3D,4D,CLRN,CK,4QN,4Q, 3QN,3Q,2QN,2Q,1QN, 1Q)

EPLDs: EP310, EP600, EP610 EP900, EP910 EP1210, EP1800, EPB1400

Default Signal Levels: GND — 1D,2D,3D,4D,CK
VCC — CLRN

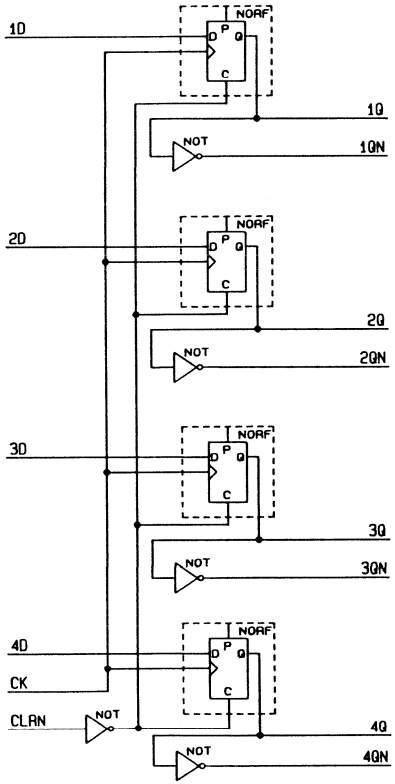
Function Table:

74175 Function Table

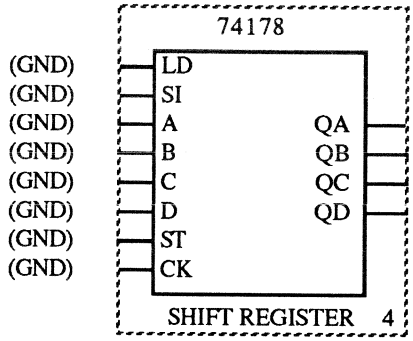
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	⌐	H	H	L
H	⌐	L	L	H
H	L	X	Q0	Q0

H = high level (steady state)
L = low level (steady state)
⌐ = transition from low to high
X = don't care
Q0 = level of Q before the indicated steady-state input conditions were established

74175 Logic Schematic:



74178 (Register)



Name: **74178** (4-Bit Shift Register)

Declaration: 74178(LD,SI,A,B,C,D,ST,CK,QD,QC,QB,QA)

EPLDs: All

Default Signal Levels: GND — all input pins

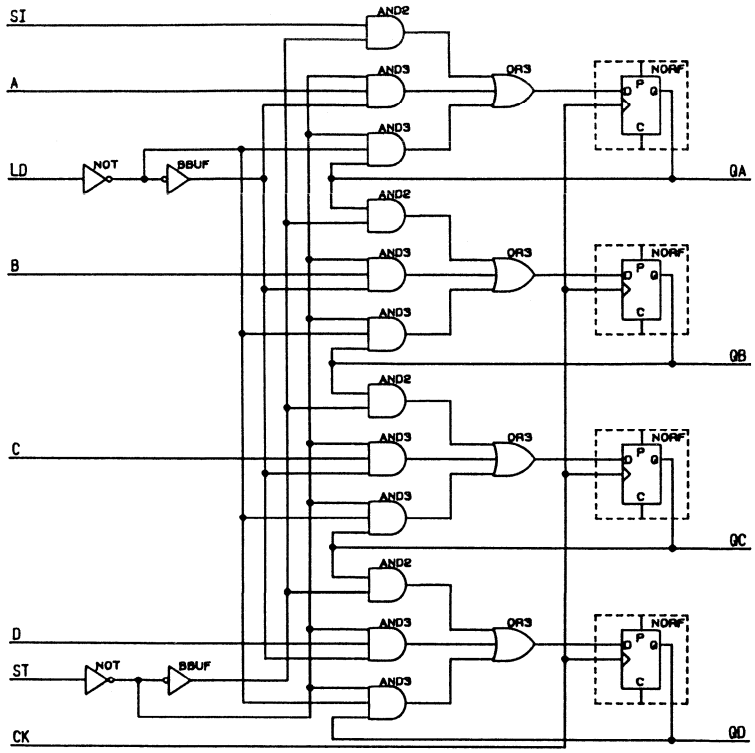
74178 Function Table:

74178 Function Table

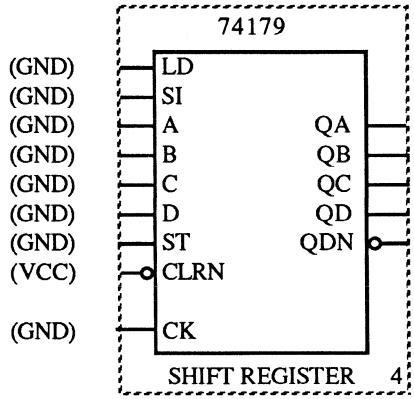
INPUTS								OUTPUTS			
SHIFT	LOAD	SI	CLOCK	PARALLEL A	B	C	D	Q_A	Q_B	Q_C	Q_D
X	X	X	L	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	L	X	⌐	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	H	X	⌐	a	b	c	d	a	b	c	d
H	X	H	⌐	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	X	L	⌐	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}

H = high level (steady state)
L = low level (steady state)
⌐ = transition from low to high level
X = don't care (any input, including transitions)
Q_{A0} ... Q_{D0} = level of Q before the indicated steady-state input conditions were established
Q_{An} ... Q_{Cn} = level of Q before the most recent active transition indicated by ⌐

74178 Logic Schematic:



74179 (Shift Register)



Name: **74179** (4-Bit Shift Register With Clear)

Declaration: 74179(LD,SI,A,B,C,D,ST,CLRN,CK,QDN, QN,QC,QB,QA)

EPLDs: EP310, EP600, EP610 EP900, EP910 EP1210, EP1800, EPB1400

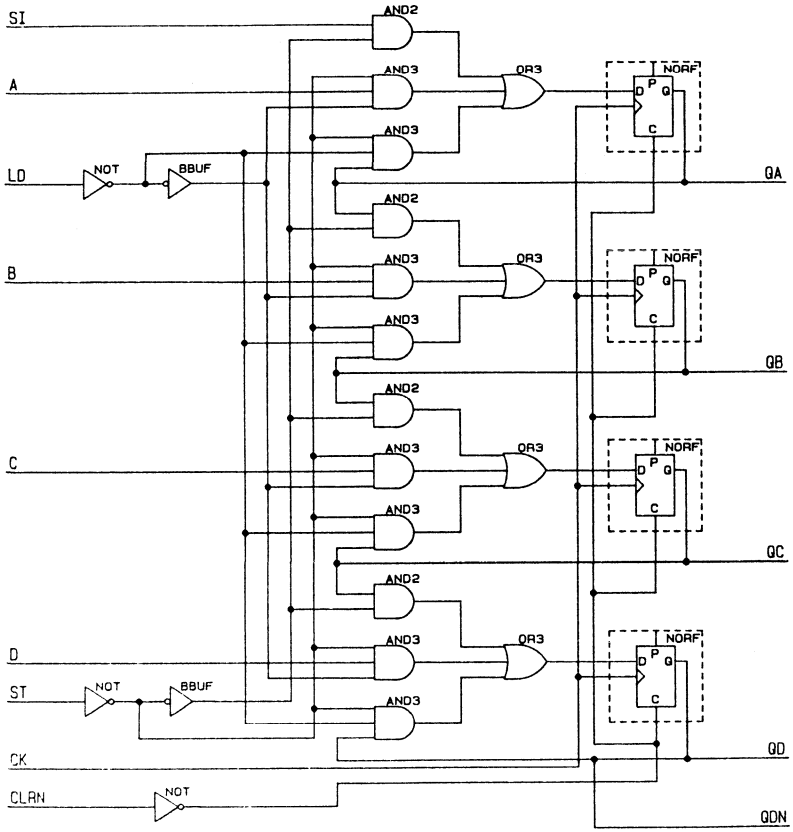
Default Signal Levels: GND — LD, SI, A, B, C, D, ST, CK
VCC — CLRN

74179 Function Table

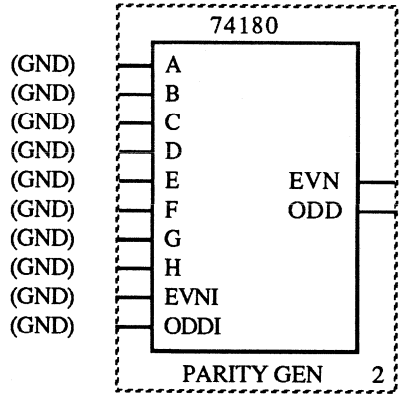
INPUTS									OUTPUTS				
CLEAR	SHIFT	LOAD	CLOCK	SI	PARALLEL A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	X	X	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	L	L	⌐	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	L	H	⌐	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	X	⌐	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	X	⌐	L	X	X	X	X	L	Q An	Q Bn	Q Cn	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
⌐ = transition from low to high level
X = don't care (any input, including transitions)
Q_{A0} to Q_{D0} = level of Q before the indicated steady-state input conditions were established
Q_n = level of Q before the most recent active transition indicated by ⌐

74179 Logic Schematic:



74180 (Parity Generator/Checker)



Name: **74180** (9-Bit Odd/Even Parity Generator/Checker)

Declaration: 74180(A,B,C,D,E,F,G,H,EVNI,ODDI,ODD, EVN)

EPLDs: All

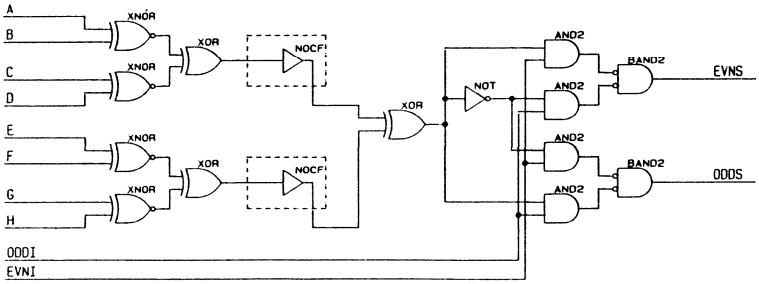
Default Signal Levels: GND — all input pins

Function Table:

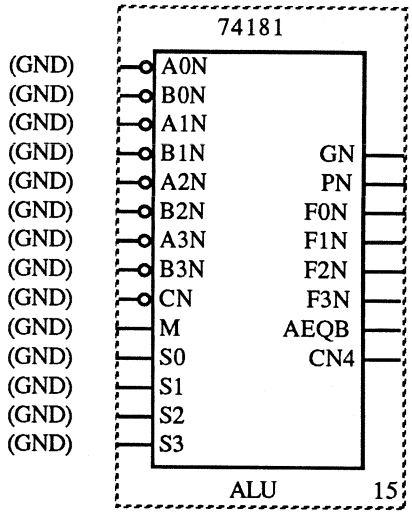
74180 Function Table

INPUTS			OUTPUTS		H = high level L = low level X = don't care
Σ OF H's AT A THROUGH H	EVNI	ODDI	Σ EVNS	Σ ODDS	
EVEN	H	L	H	L	
ODD	H	L	L	H	
EVEN	L	H	L	H	
ODD	L	H	H	L	
X	H	H	L	L	
X	L	L	H	H	

74180 Logic Schematic:



74181 (Arithmetic Logic Unit)



Name: **74181** (Arithmetic Logic Unit)

Declaration: 74181(A0N,B0N,A1N,B1N,A2N,B2N,A3N, B3N,CN,M,S0,S1,S2,S3,CN4,AEQB,F3N, F2N,F1N,F0N,PN,GN)

EPLDs: EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

74181 Function Table (Table 1)

SELECTION				ACTIVE LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A} + B$	F = $A\overline{B}$ MINUS 1	F = $A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2s COMP)	F = ZERO
L	H	L	L	$F = \overline{A+B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	$F = \overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + B) PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	$F = \overline{A}B$	F = A PLUS (A+B)	F = A PLUS (A+B) PLUS 1
H	L	L	H	$F = A \oplus B'$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = $A\overline{B}$ PLUS (A + B)	F = $A\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB + A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = $A\overline{B}$ + A	F = $A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

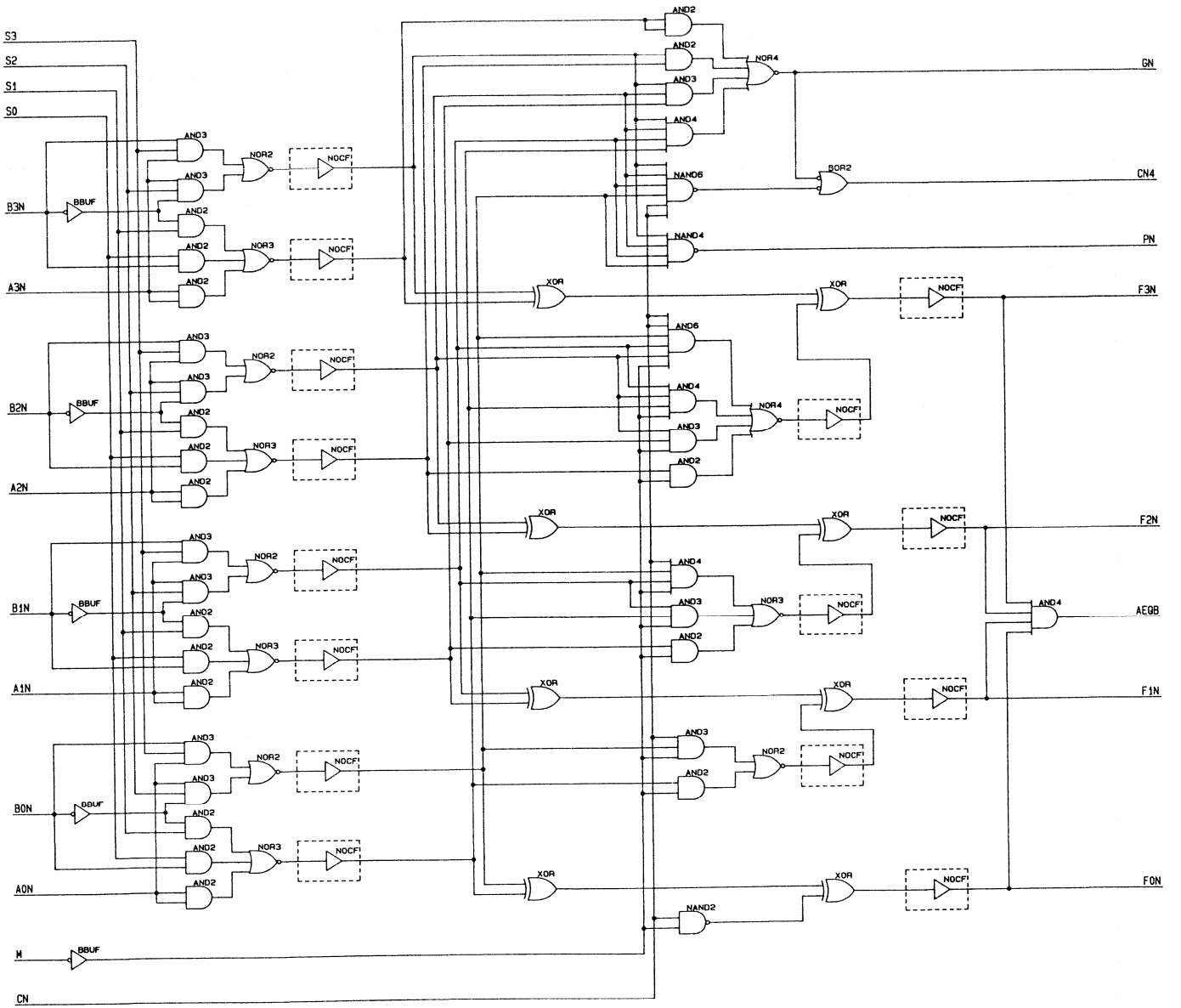
H = high level (steady state)
L = low level (steady state)
* Each bit is shifted to the next more significant position

74181 Function Table (Table 2)

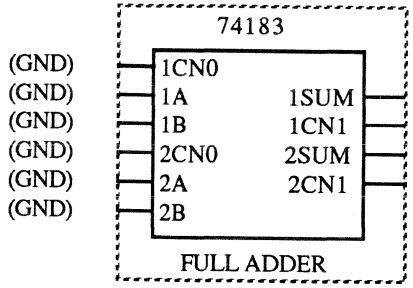
SELECTION				ACTIVE HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2s COMP)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS AB	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = A + B PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A$\oplus$B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A + B}$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = A$\oplus$B'	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A + $\overline{B}$ PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

H = high level (steady state)
L = low level (steady state)
* Each bit is shifted to the next more significant position

74181 Logic Schematic:



74183 (Full Adder)



Name: **74183** (Dual Carry-Save Full Adder)

Declaration: 74183(1CN0,1A,1B,2CN0,2A,2B,2CN1, 2SUM,1CN1,1SUM)

EPLDs: All

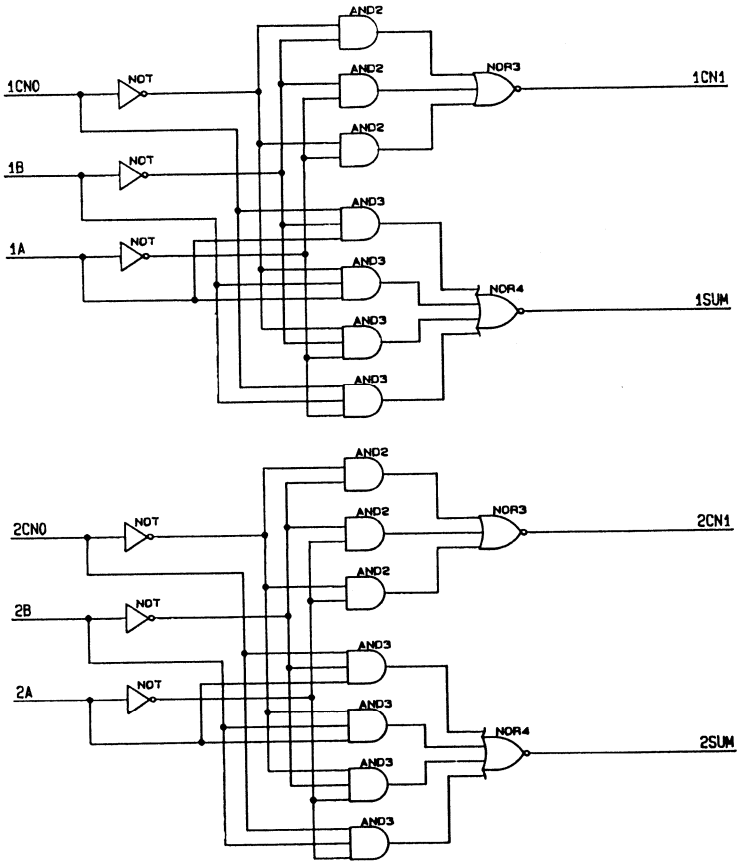
Default Signal Levels: GND — all input pins

Function Table:

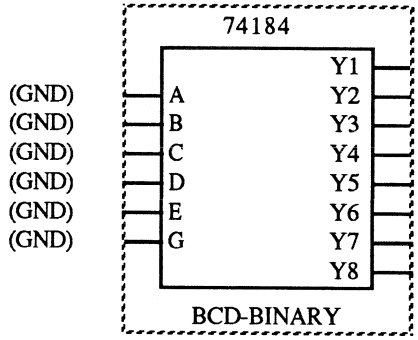
74183 Function Table

INPUTS			OUTPUTS		H = high level L = low level
CN0	B	A	SUM	CN1	
L	L	L	L	L	
L	L	H	H	L	
L	H	L	H	L	
L	H	H	L	H	
H	L	L	H	L	
H	L	H	L	H	
H	H	L	L	H	
H	H	H	H	H	

74183 Logic Schematic:



74184 (Converter)



Name: **74184** (BCD-to-Binary Converter)

Declaration: 74184(A,B,C,D,E,G,Y1,Y2,Y3,Y4,Y5,Y6, Y7,Y8)

EPLDs: All

Default Signal Levels: GND — all input pins

74184 Function Table (1):

74184 Function Table (BCD to Binary Converter)

BCD WORDS	INPUTS						OUTPUTS				
	E	D	C	B	A	G	Y5	Y4	Y3	Y2	Y1
0-1	L	L	L	L	L	L	L	L	L	L	L
2-3	L	L	L	L	H	L	L	L	L	L	H
4-5	L	L	L	H	L	L	L	L	L	H	L
6-7	L	L	L	H	H	L	L	L	L	H	H
8-9	L	L	H	L	L	L	L	L	H	L	L
10-11	L	H	L	L	L	L	L	L	H	L	H
12-13	L	H	L	L	H	L	L	L	H	H	L
14-15	L	H	L	H	L	L	L	L	H	H	H
16-17	L	H	L	H	H	L	L	H	L	L	L
18-19	L	H	H	L	L	L	L	H	L	L	H
20-21	H	L	L	L	L	L	L	H	L	H	L
22-23	H	L	L	L	H	L	L	H	L	H	H
24-25	H	L	L	H	L	L	L	H	H	L	L
26-27	H	L	L	H	H	L	L	H	H	L	H
28-29	H	L	H	L	L	L	L	H	H	L	L
30-31	H	H	L	L	L	L	L	H	H	H	H
32-33	H	H	L	L	H	L	H	L	L	L	L
34-35	H	H	L	H	L	L	H	L	L	L	H
36-37	H	H	L	H	H	L	H	L	L	H	L
38-39	H	H	H	L	L	L	H	L	L	H	H
ANY	X	X	X	X	X	H	H	H	H	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
Input conditions other than those shown produce high levels at outputs Y1 to Y5.
Outputs Y6, Y7, and Y8 are not used for BCD to binary conversion

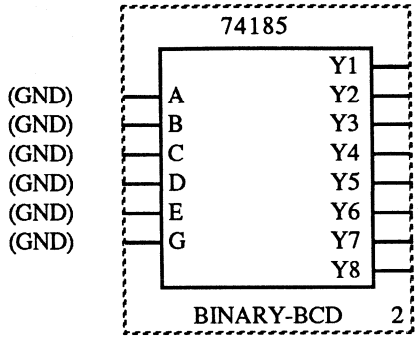
74184 Function Table (2):

74184 Function Table
(BCD 9s or BCD 10s Complement)

BCD WORDS	INPUTS						OUTPUTS		
	E*	D	C	B	A	G	Y6	Y7	Y8
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	L	L	L	H	L
6	L	L	H	H	H	L	L	L	H
7	L	L	H	H	L	L	L	L	L
8	L	H	L	L	H	L	L	L	H
9	L	H	L	L	L	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	L	L	L	H	L
6	H	L	H	H	H	L	L	H	L
7	H	L	H	H	L	L	L	L	H
8	H	H	L	L	H	L	L	L	H
9	H	H	L	L	L	L	L	L	L
ANY	X	X	X	X	X	H	H	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
Input conditions other than those shown produce high levels at outputs Y6, Y7, and Y8.
Outputs Y1 through Y5 are not used for BCD 9s or 10s complement conversion.
* When these devices are used as complement converters, input E is used as a mode control.

74185 (Converter)



Name: **74185** (Binary-to-BCD Converter)

Declaration: 74185(A,B,C,D,E,G,Y1,Y2,Y3,Y4,Y5,Y6, Y7,Y8)

EPLDs: EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

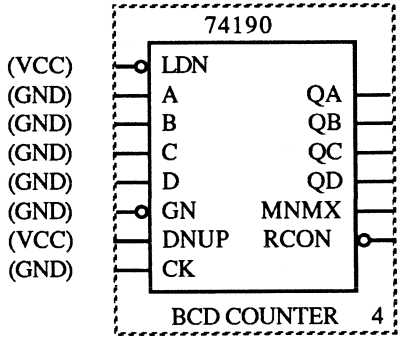
74185 Function Table:

74185 Function Table (Binary to BCD Converter)

BCD WORDS	INPUTS						OUTPUTS							
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0-1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2-3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4-5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6-7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8-9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10-11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12-13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14-15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16-17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18-19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20-21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22-23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24-25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26-27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28-29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30-31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32-33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34-35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36-37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38-39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40-41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42-43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44-45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46-47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48-49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50-51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52-53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54-55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56-57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58-59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60-61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62-63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)

74190 (Counter)



Name: **74190** (4-Bit Up/Down Decade Counter With Synchronous Load)

Declaration: 74190(GN,LDN,DNUP,A,B,C,D,CK,QD, QC,QB,QA,MNMX,RCON)

EPLDs: All

Default Signal Levels: GND — A, B, C, D, CK, GN
VCC — LDN, DNUP

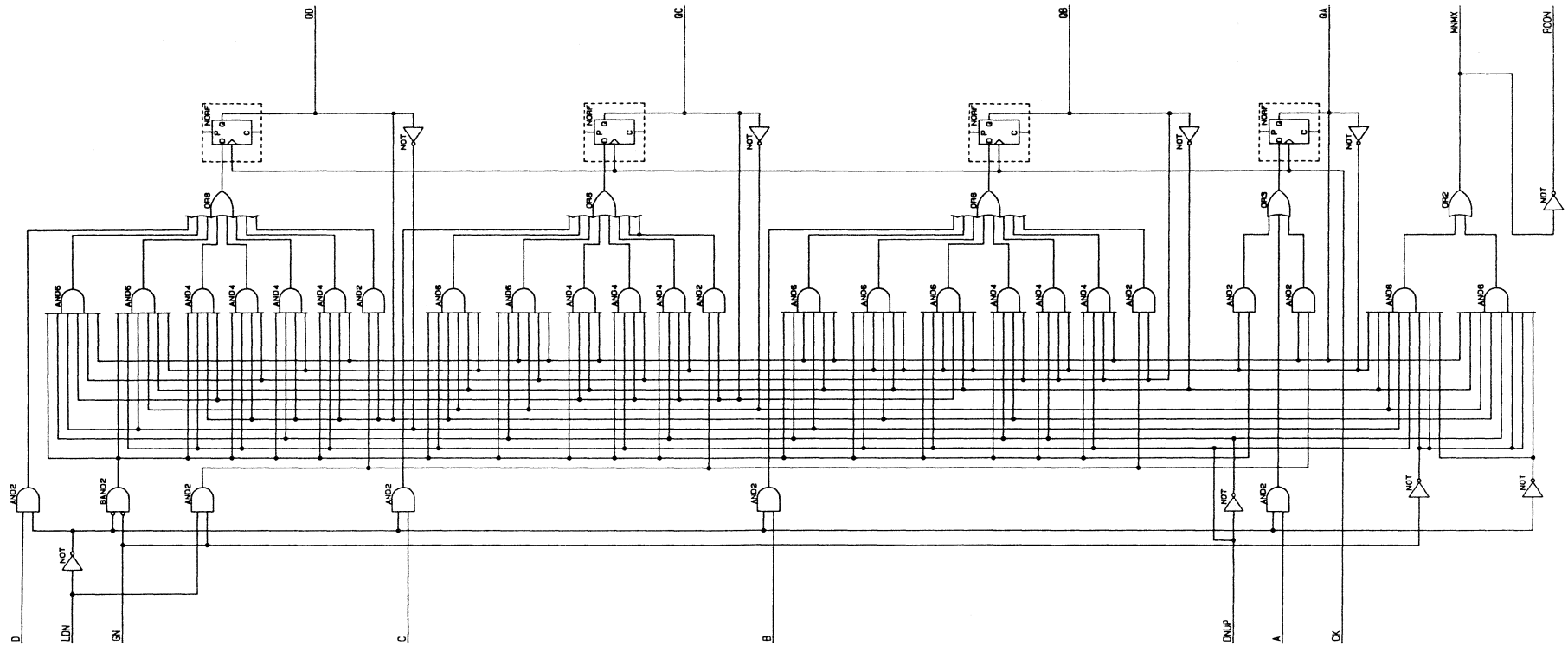
74190 Function Table:

74190 Function Table

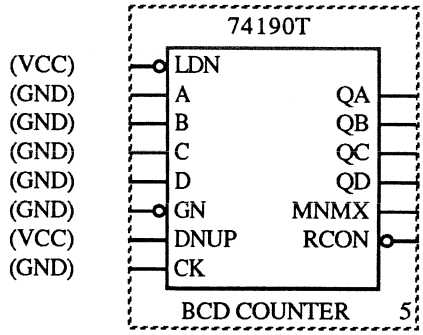
INPUTS								OUTPUTS					
CK	GN	LDN	DNUP	D	C	B	A	Q_D	Q_C	Q_B	Q_A	MNMX	RCON
⌐	X	L	X	d	c	b	a	d	c	b	a	X	X
X	L	H	L					H	L	L	H	H	L
X	L	H	H					L	L	L	L	H	L
⌐	L	H	L					COUNT UP				L	H
⌐	L	H	H					COUNT DOWN				L	H
⌐	H	H	X					HOLD COUNT				L	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74190 Logic Schematic:



74190T (Counter)



Name: **74190T** (4-Bit Up/Down Decade Counter)

Declaration: 74190T(LDN,A,B,C,D,GN,DNUP,CK, RCON,MNMX,QD,QC,QB,QA)

EPLDs: EP600, EP610, EP900, EP910, EP1800, EPB1400

Default Signal Levels: GND — A, B, C, D, CK, GN
VCC — LDN, DNUP

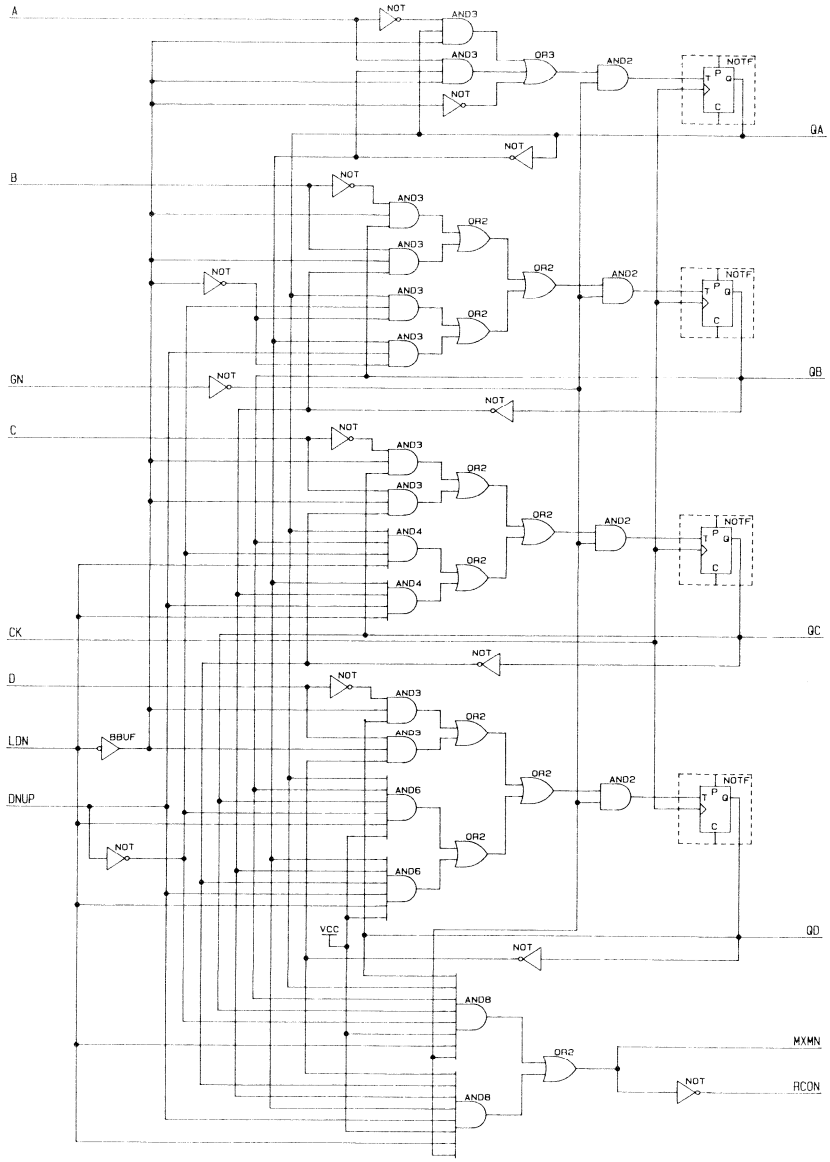
74190T Function Table:

74190T Function Table

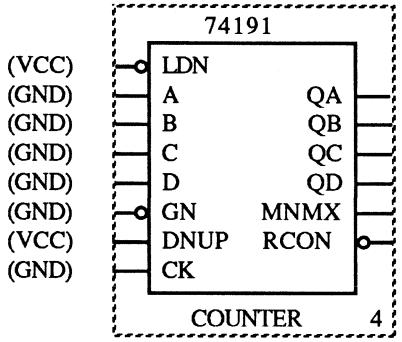
INPUTS								OUTPUTS					
CK	GN	LDN	DNUP	D	C	B	A	Q_D	Q_C	Q_B	Q_A	MNMX	RCON
⌐	X	L	X	d	c	b	a	d	c	b	a	X	X
X	L	H	L					H	L	L	H	H	L
X	L	H	H					L	L	L	L	H	L
⌐	L	H	L					COUNT UP				L	H
⌐	L	H	H					COUNT DOWN				L	H
⌐	H	H	X					HOLD COUNT				L	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74190T Logic Schematic:



74191 (Counter)



Name: **74191** (4-Bit Binary Up/Down Counter With Synchronous Load)

Declaration: 74191(GN,LDN,DNUP,A,B,C,D,CK,QD, QC,QB,QA,MNMX,RCON)

EPLDs: All

Default Signal Levels: GND — A, B, C, D, CK, GN
VCC — LDN, DNUP

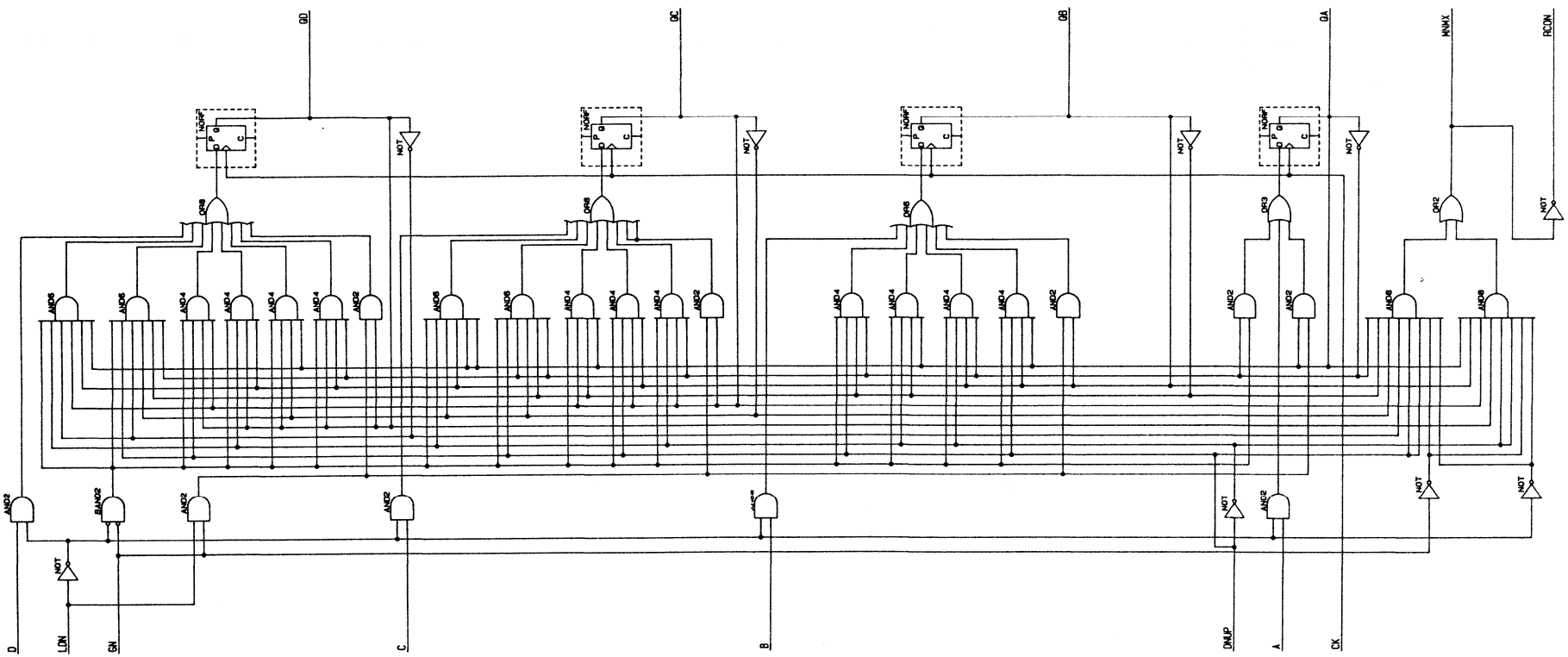
74191 Function Table:

74191 Function Table

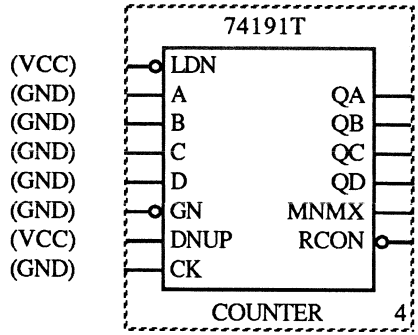
INPUTS								OUTPUTS					
CK	GN	LDN	DNUP	D	C	B	A	Q_D	Q_C	Q_B	Q_A	MNMX	RCON
⌐	X	L	X	d	c	b	a	d	c	b	a	X	X
X	L	H	L					H	H	H	H	H	L
X	L	H	H					L	L	L	L	H	L
⌐	L	H	L					COUNT UP				L	H
⌐	L	H	H					COUNT DOWN				L	H
⌐	H	H	X					HOLD COUNT				L	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74191 Logic Schematic:



74191T (Counter)



Name: **74191T** (4-Bit Binary Up/Down Counter)

Declaration: 74191T(LDN,A,B,C,D,GN,DNUP,CK, RCON,MNMX,QD,QC,QB,QA)

EPLDs: EP600, EP610, EP900, EP910, EP1800, EPB1400

Default Signal Levels: GND — A, B, C, D, CK, GN
VCC — LDN, DNUP

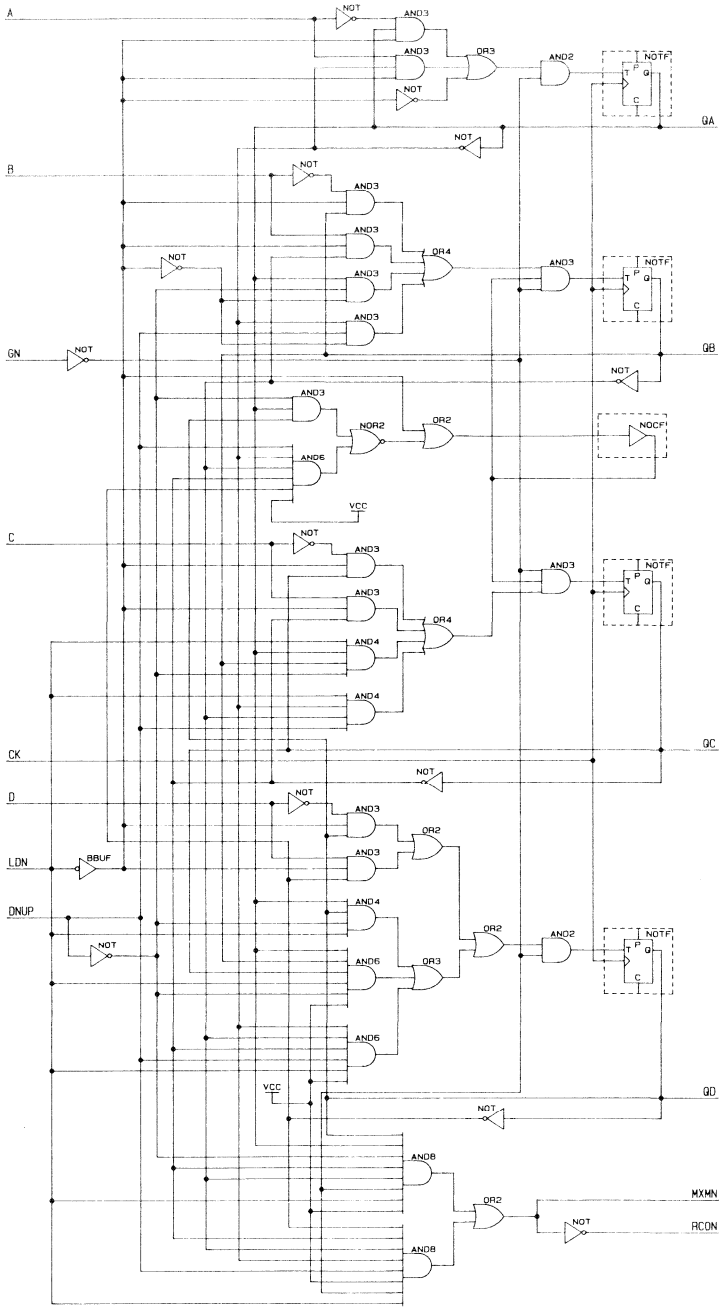
74191T Function Table:

74191T Function Table

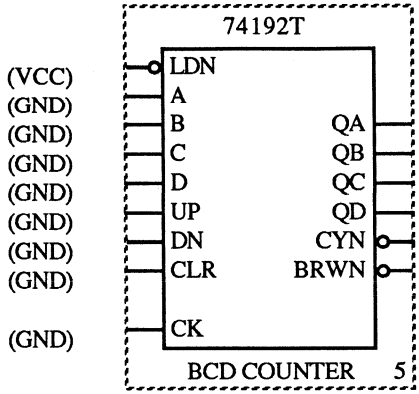
INPUTS								OUTPUTS					
CK	GN	LDN	DNUP	D	C	B	A	Q_D	Q_C	Q_B	Q_A	MNMX	RCON
⌐	X	L	X	d	c	b	a	d	c	b	a	X	X
X	L	H	L					H	H	H	H	H	L
X	L	H	H					L	L	L	L	H	L
⌐	L	H	L					COUNT UP				L	H
⌐	L	H	H					COUNT DOWN				L	H
⌐	H	H	X					HOLD COUNT				L	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74191T Logic Schematic:



74192T (Counter)



Name: **74192T** (4-Bit Up/Down Decade Counter With Clear)

Declaration: 74192T(LDN,A,B,C,D,UP,DN,CLR,CK, BRWN,CYN,QD,QC,QB,QA)

EPLDs: EP600, EP610, EP900, EP910, EP1800, EPB1400

Default Signal Levels: GND — A, B, C, D, UP, DN, CLR, CK
VCC — LDN

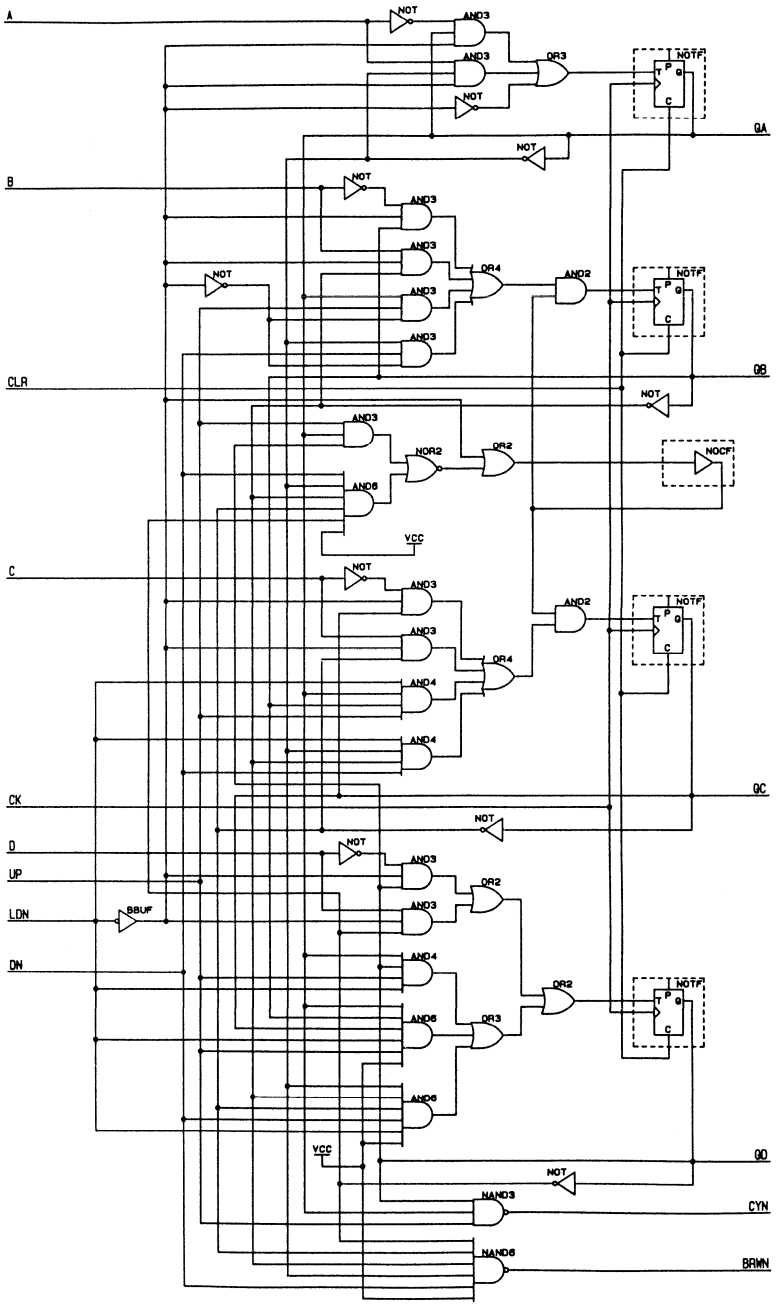
74192T Function Table:

74192T Function Table

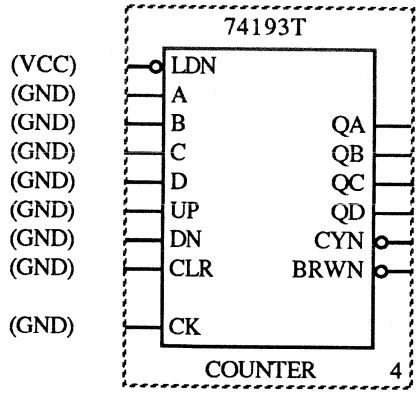
INPUTS									OUTPUTS					
CLR	CK	LDN	UP	DN	D	C	B	A	Q_D	Q_C	Q_B	Q_A	CARRY CYN	BORROW BRWN
H	X	X	X	L	X	X	X	X	L	L	L	L	H	H
H	X	X	X	H	X	X	X	X	L	L	L	L	H	L
L	⌐	L	X	X	d	c	b	a	d	c	b	a	H	H
L	⌐	H	H	L	X	X	X	X	COUNT UP				H	H
L	⌐	H	L	H	X	X	X	X	COUNT DOWN				H	H
L	⌐	H	L	L	X	X	X	X	HOLD COUNT				H	H
L	⌐	H	H	H	X	X	X	X	ILLEGAL				X	X
L	X	H	H	L	X	X	X	X	H	L	L	H	L	H
L	X	H	L	H	X	X	X	X	L	L	L	L	H	L

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74192T Logic Schematic:



74193T (Counter)



Name: **74193T** (4-Bit Up/Down Binary Counter With Clear)

Declaration: 74193T(LDN,A,B,C,D,UP,DN,CLR,CK, BRWN,CYN,QD,QC,QB,QA)

EPLDs: EP600, EP610, EP900, EP910, EP1800, EPB1400

Default Signal Levels: GND — A, B, C, D, UP, DN, CLR, CK
VCC — LDN

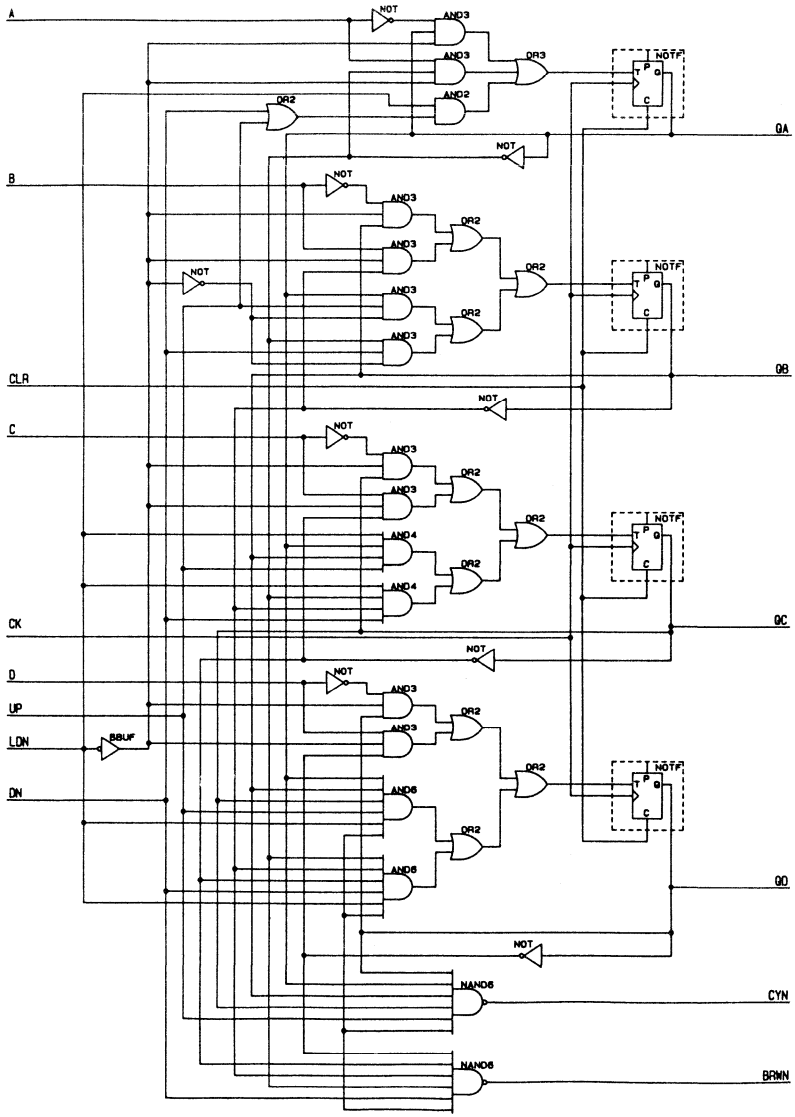
74193T Function Table:

74193T Function Table

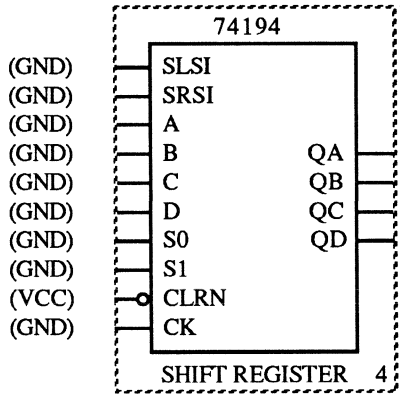
INPUTS									OUTPUTS					
CLR	CK	LDN	UP	DN	D	C	B	A	Q_D	Q_C	Q_B	Q_A	CARRY CYN	BORROW BRWN
H	X	X	X	L	X	X	X	X	L	L	L	L	H	H
H	X	X	X	H	X	X	X	X	L	L	L	L	H	L
L	⌐	L	X	X	d	c	b	a	d	c	b	a	H	H
L	⌐	H	H	L	X	X	X	X	COUNT UP				H	H
L	⌐	H	L	H	X	X	X	X	COUNT DOWN				H	H
L	⌐	H	L	L	X	X	X	X	HOLD COUNT				H	H
L	⌐	H	H	H	X	X	X	X	ILLEGAL				X	X
L	X	H	H	L	X	X	X	X	H	H	H	H	L	H
L	X	H	L	H	X	X	X	X	L	L	L	L	H	L

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D

74193T Logic Schematic:



74194 (Shift Register)



Name: **74194** (4-Bit Bi-Directional Shift Register With Parallel Load)

Declaration: 74194(SLSI,SRSI,A,B,C,D,R,S0,S1, CLRN,CK,QD,QC,QB,QA)

EPLDs: EP310, EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — SLSI,SRSI, A, B, C, D, S0, S1, CK
VCC — CLRN

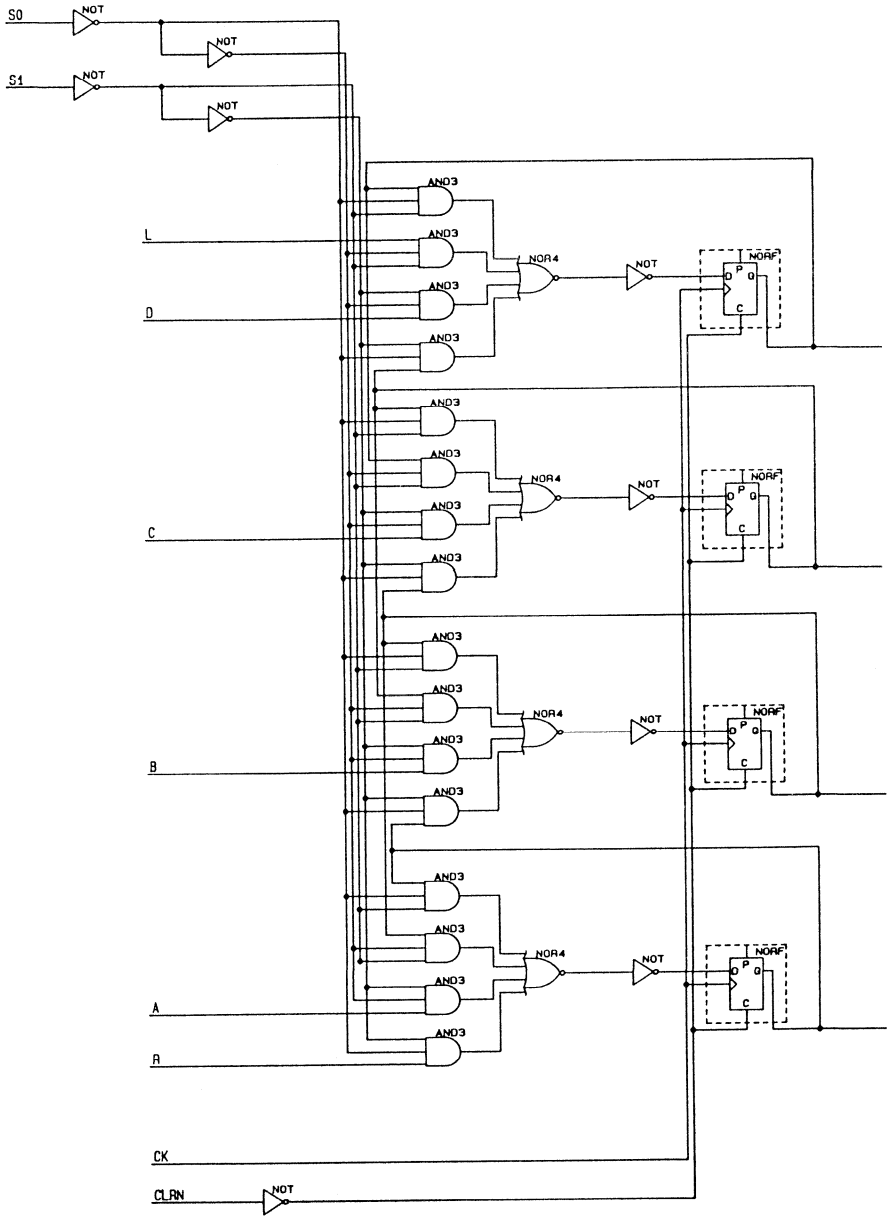
74194 Function Table:

74194 Function Table

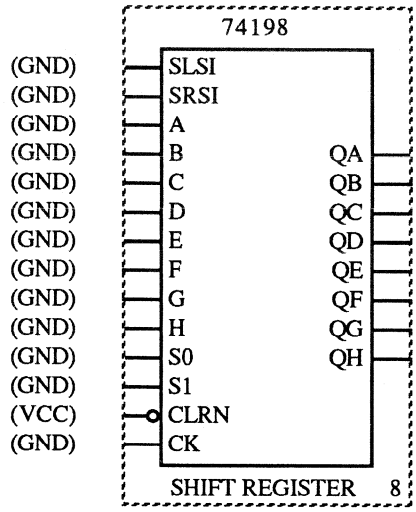
INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		L	R	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	⌐	X	X	a	b	c	d	a	b	c	d
H	L	H	⌐	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	⌐	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	⌐	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	⌐	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	⌐	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D
Q_{A0} Q_{B0} Q_{C0} Q_{D0} = level of Q_A Q_B Q_C Q_D before the indicated steady-state input conditions were established
Q_{An} Q_{Bn} Q_{Cn} Q_{Dn} = level of Q_A Q_B Q_C Q_D before the most recent ⌐ transition of the clock

74194 Logic Schematic:



74198 (Shift Register)



Name: **74198** (8-Bit Bi-Directional Shift Register)

Declaration: 74198(SLSI,SRSI,A,B,C,D,E,F,G,H,S0, S1,CLRN,CK,QH,QG,QF,QE,QD,QC,QB,QA)

EPLDs: EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — SLSI, SRSI, A, B, C, D, E, F, G, H, S0, S1, CK
VCC — CLRN

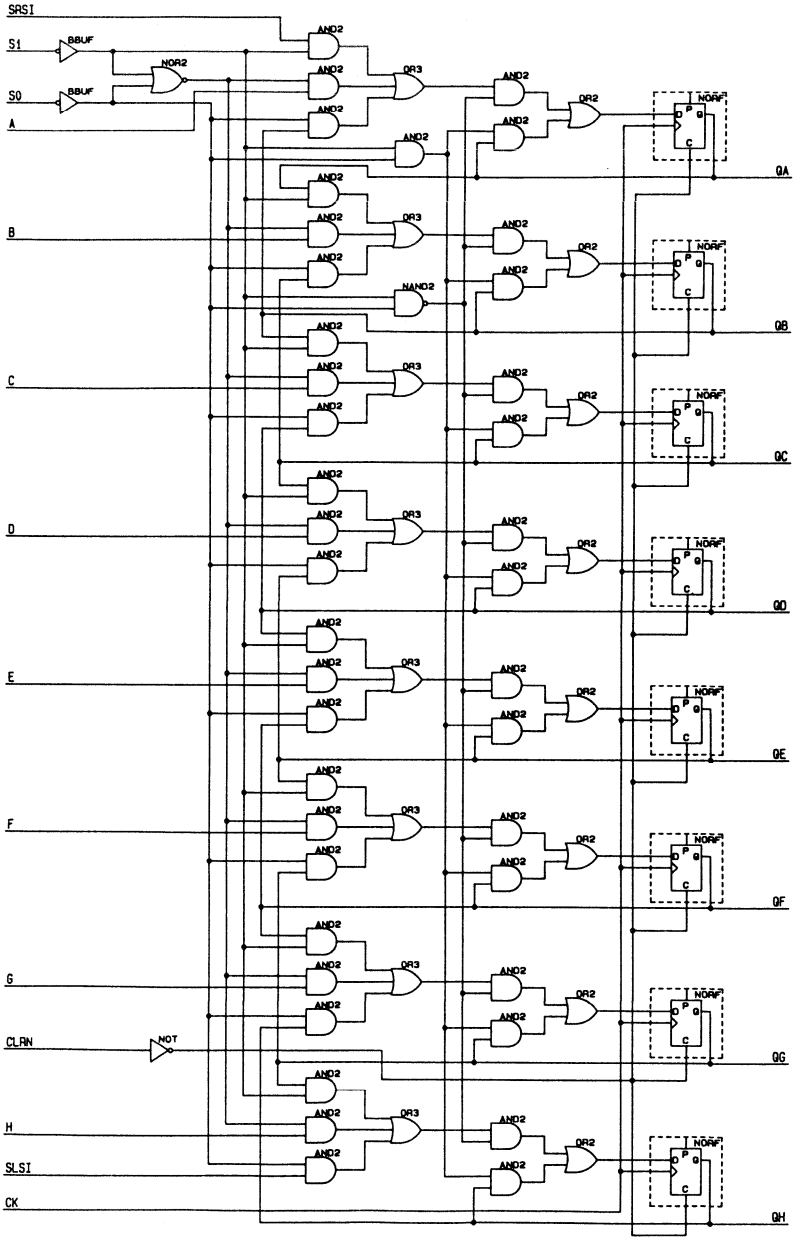
74198 Function Table:

74198 Function Table

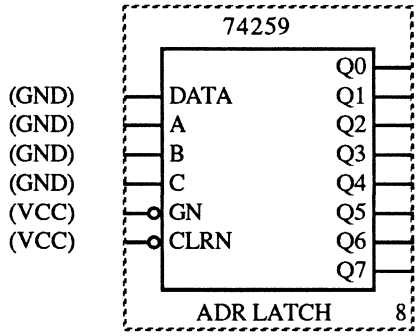
INPUTS							OUTPUTS			
CLEAR	MODE S1	MODE S0	CLOCK	SLSI	SRSI	PARALLEL A ... H	Q_A	Q_B ...	Q_G	Q_H
L	X	X	X	X	X	X	L	L	L	L
H	H	H	⌐¬	X	X	a ...h	a	b	g	h
H	L	H	⌐¬	X	H	X	H	Q_{An}	Q_{Fn}	Q_{Gn}
H	L	H	⌐¬	X	L	X	L	Q_{An}	Q_{Fn}	Q_{Gn}
H	H	L	⌐¬	H	X	X	Q_{Bn}	Q_{Cn}	Q_{Hn}	H
H	H	L	⌐¬	L	X	X	Q_{Bn}	Q_{Cn}	Q_{Hn}	L
H	L	L	X	X	X	X	Q_{A0}	Q_{B0}	Q_{G0}	Q_{H0}

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
⌐¬ = transition from low to high level
a,b,c,d, = level of steady state input at inputs A,B,C,D
Q_{A0} ... Q_{H0} = level of Q_A to Q_D before the indicated steady-state input conditions were established
Q_{An} to Q_{Hn} = level of Q_A to Q_H before the most recent ⌐¬ transition of the clock

74198 Logic Schematic:



74259 (Latch)



Name: **74259** (8-Bit Addressable Latch With Clear)

Declaration: 74259(DATA,A,B,C,GN,CLRN,Q7,Q6,Q5, Q4,Q3,Q2,Q1,Q0)

EPLDs: All

Default Signal Levels: GND — DATA, A, B, C
VCC — GN CLRN

74259 Function Table:

74259 Function Table

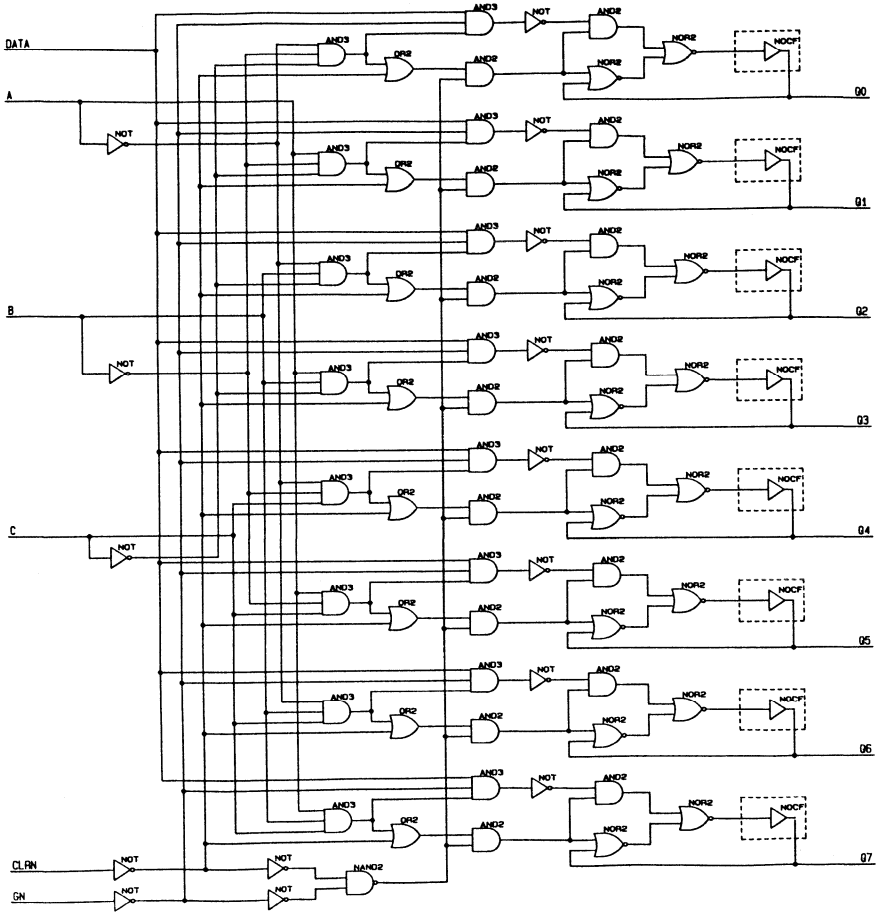
INPUTS		OUTPUTS		FUNCTION
CLEAR	$\overline{G}$	ADDRESSED LATCH	OTHER LATCHES	
H	L	DATA	Q_{io}	ADDRESSABLE LATCH
H	H	Q_{io}	Q_{io}	MEMORY
L	L	DATA	L	8-LINE DEMUX
L	H	L	L	CLEAR

H = high level
L = low level
Q_{io} = level of Q_i (i = 0 ...7) before indicated steady-state input conditions were established.

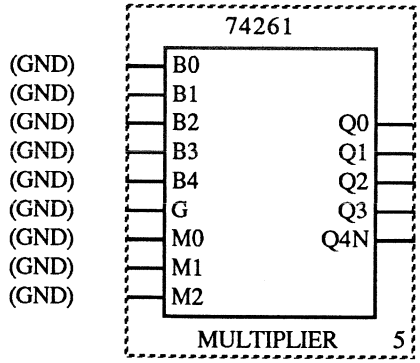
Latch Selection Table

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

74259 Logic Schematic:



74261 (Multiplier)



Name: **74261** (2-Bit Parallel Binary Multiplier)

Declaration: 74261(B0,B1,B2,B3,B4,G,M0,M1,M2, Q4N,Q3,Q2,Q1,Q0)

EPLDs: All

Default Signal Levels: GND — all input pins

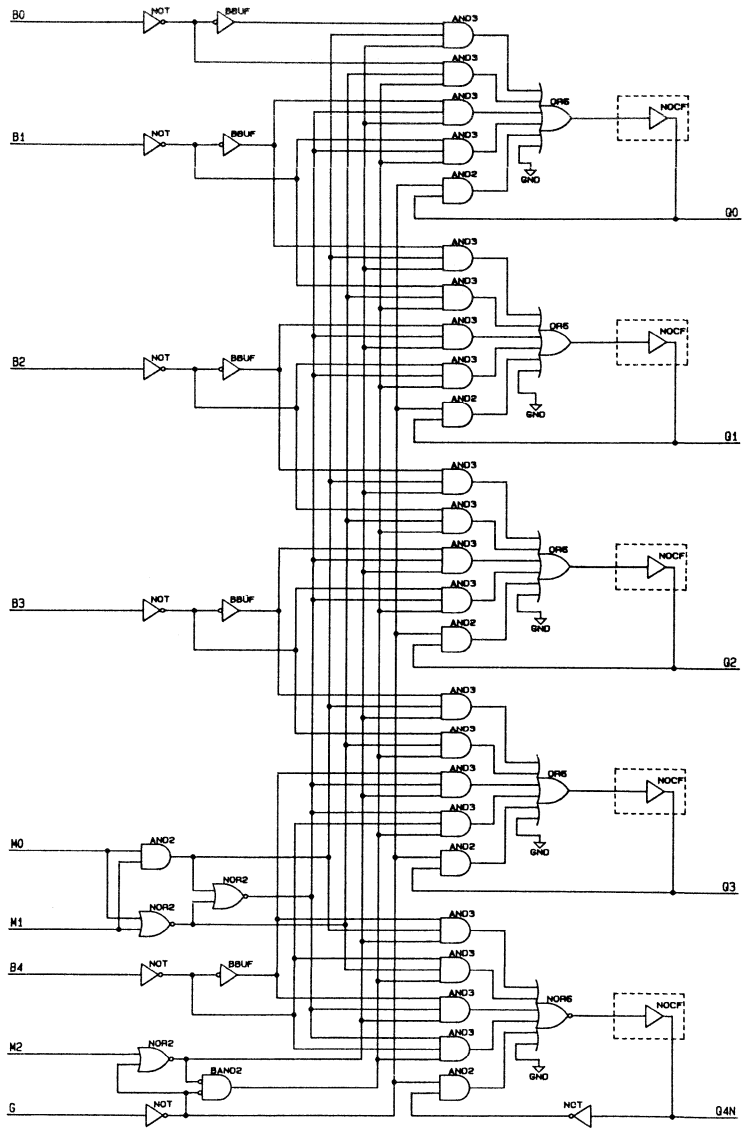
74261 Function Table:

74261 Function Table

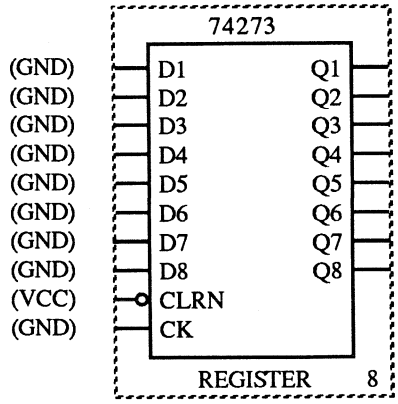
INPUTS				OUTPUTS				
LATCH CONTROL G	MULTIPLIER			$\overline{Q}4$	Q3	Q2	Q1	Q0
	M2	M1	M0					
L	X	X	X	$\overline{Q}4_0$	$Q3_0$	$Q2_0$	$Q1_0$	$Q0_0$
H	L	L	L	H	L	L	L	L
H	L	L	H	$\overline{B}4$	B4	B3	B2	B1
H	L	H	L	$\overline{B}4$	B4	B3	B2	B1
H	L	H	H	$\overline{B}4$	B3	B2	B1	B0
H	H	L	L	B4	$\overline{B}3$	$\overline{B}2$	$\overline{B}1$	$\overline{B}0$
H	H	L	H	B4	$\overline{B}4$	$\overline{B}3$	$\overline{B}2$	$\overline{B}1$
H	H	H	L	B4	$\overline{B}4$	$\overline{B}3$	$\overline{B}2$	$\overline{B}1$
H	H	H	H	H	L	L	L	L

H = high level
L = low level
X = don't care
$\overline{Q}4_0$ ... $Q0_0$ = the logic levelof the same output before the high-to-low transition of G
B4 ... B0 = the logic level of the indicated multiplicand (B) input

74261 Logic Schematic:



74273 (Register)



Name: **74273** (Octal D-Type Flipflop With Asynchronous Clear)

Declaration: 74273(D1,D2,D3,D4,D5,D6,D7,D8,CLRN, CK,Q8,Q7,Q6,Q5,Q4,Q3,Q2,Q1)

EPLDs: EP310, EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — D1, D2, D3, D4, D5, D6, D7, D8, CK
VCC — CLRN

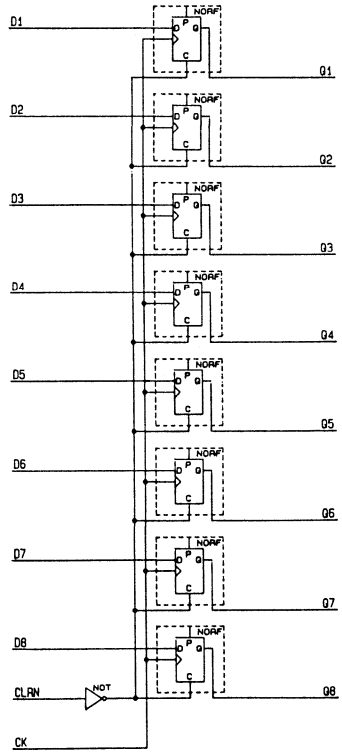
74273 Function Table:

74273 Function Table (each flipflop)

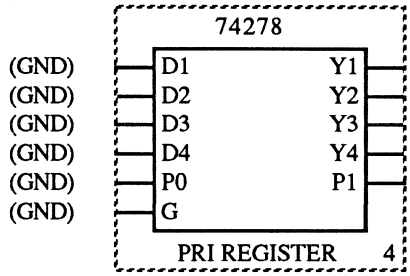
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = high level (steady state)
L = low level (steady state)
X = don't care
Q_0 = level of Q before the indicated steady-state input conditions were established
↑ = transition from low to high

74273 Logic Schematic:



74278 (Storage Register)



Name: **74278** (4-Bit Cascadable Priority Register)

Declaration: 74278(D1,D2,D3,D4,P0,G,P1,Y4,Y3,Y2,Y1)

EPLDs: All

Default Signal Levels: GND — all input pins

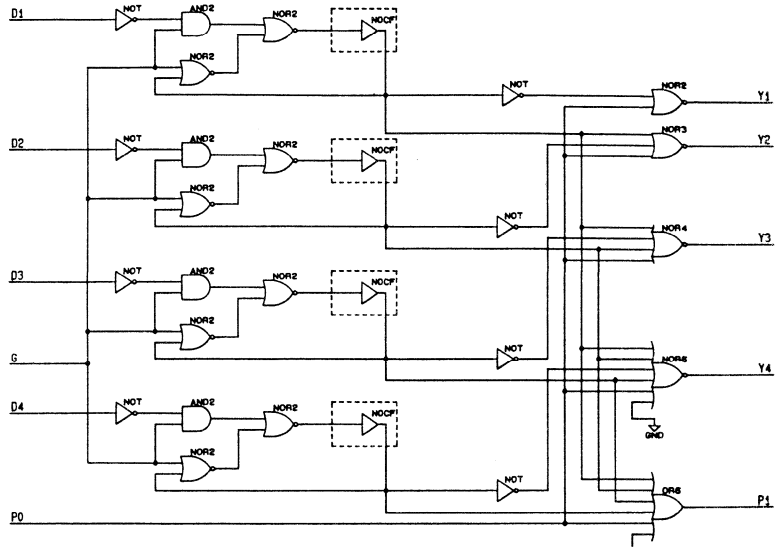
74278 Function Table:

74278 Function Table

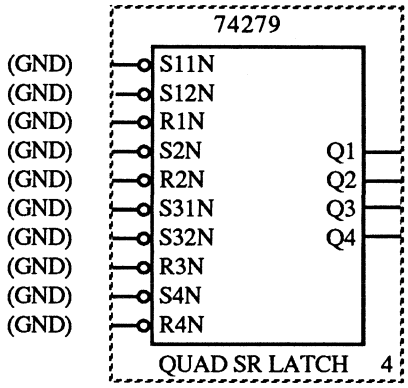
INPUTS						INTERNAL LATCH NODES				OUTPUTS				
P0	G	D1	D2	D3	D4	$\overline{Q}1$	$\overline{Q}2$	$\overline{Q}3$	$\overline{Q}4$	Y1	Y2	Y3	Y4	P1
L	H	H	L	X	X	L	X	X	X	H	L	L	L	H
L	H	L	H	X	X	H	L	X	X	L	H	L	L	H
L	H	L	L	H	X	H	H	L	X	L	L	H	L	H
L	H	L	L	L	H	H	H	H	L	L	L	L	H	H
L	H	L	L	L	L	H	H	H	H	L	L	L	L	L
L	L	X	X	X	X	Latched when G goes low				Same function of $\overline{Q}$ as on first 5 lines				
H	L	X	X	X	X					L	L	L	L	H
H	H	Internal $\overline{Q}$ levels are the same function of D inputs as on the first 5 lines								L	L	L	L	H

H = high level
L = low level
X = don't care

74278 Logic Schematic:



74279 (Latch)



Name: **74279** (Quad /S-/R Latch)

Declaration: 74279(S11N,S12N,R1N,S2N,R2N,S31N, S32N,R3N,S4N,R4N,Q4,Q3,Q2,Q1)

EPLDs: All

Default Signal Levels: GND— all input pins

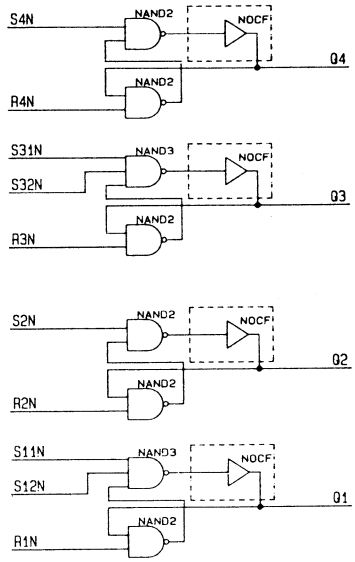
74279 Function Table:

74279 Function Table

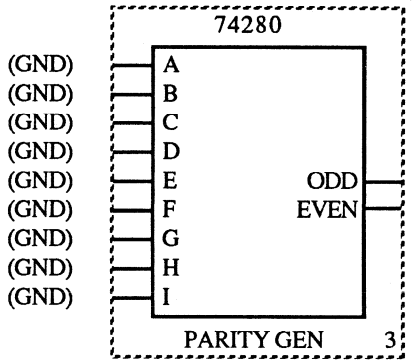
INPUTS $\overline{SN}$	INPUTS $\overline{RN}$	OUTPUT Q
H	H	Q_0*
L	H	H
H	L	L
L	L	H**

H = high level (steady state)
L = low level (steady state)
Q_0 = level of Q before the indicated input conditions were established
* This output level is pseudo stable.
** For latches with double $\overline{S}$ inputs:
H = both $\overline{SN}$ inputs high
L = one or both $\overline{SN}$ inputs low

74279 Logic Schematic:



74280 (Parity Generator/Checker)



Name: **74280** (9-Bit Odd/Even Parity Generator/Checker)

Declaration: 74280(A,B,C,D,E,F,G,H,I,EVEN,ODD)

EPLDs: All

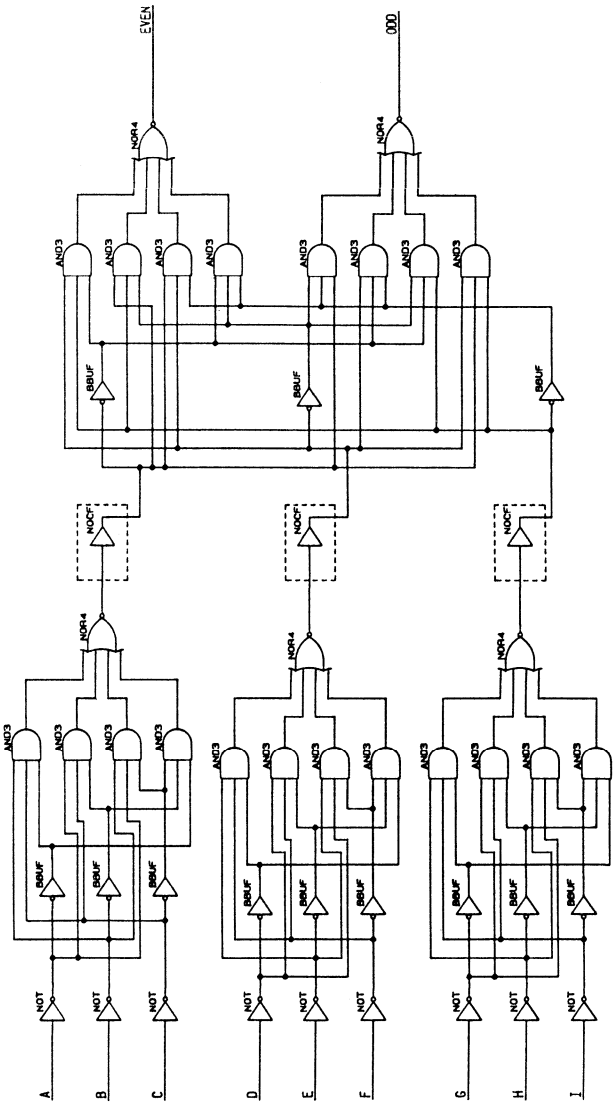
Default Signal Levels: GND — all input pins

Function Table:

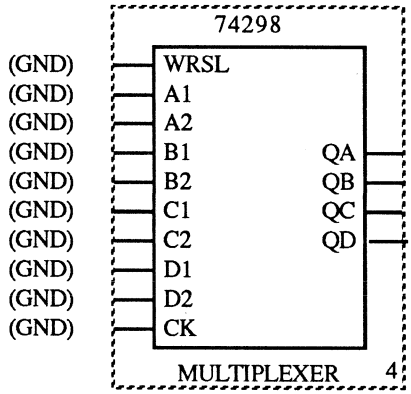
74280 Function Table

NUMBER OF INPUTS A THROUGH I THAT ARE HIGH	OUTPUTS	
	EVEN	ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

74280 Logic Schematic:



74298 (Multiplexer)



Name: **74298** (Quad 2-Input Multiplexer With Storage)

Declaration: 74298(WRSL,A1,A2,B1,B2,C1,C2,D1,D2, CK,QD,QC,QB,QA)

EPLDs: All

Default Signal Levels: GND — all input pins

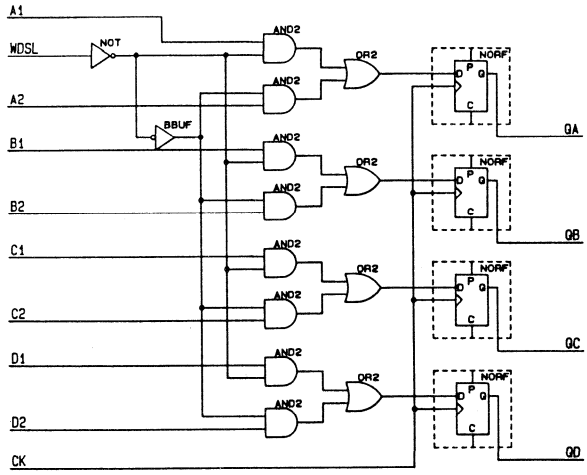
74298 Function Table:

74298 Function Table

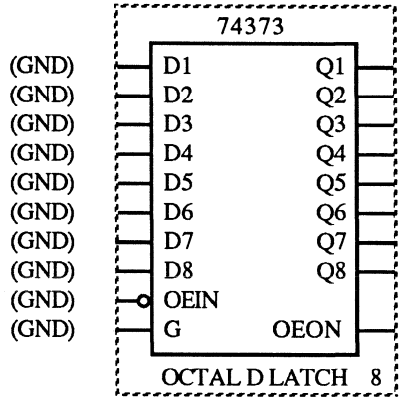
INPUTS		OUTPUTS			
WRSL	CK	Q_A	Q_B	Q_C	Q_D
L	⌐	a1	b1	c1	d1
H	⌐	a2	b2	c2	d2
X	L	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level L = low level
X = don't care
⌐ = transition from low to high
a1, a2, b1, etc. = the level of steady-state inputs at A1, A2, B1, etc.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, etc. entered on the most recent ⌐ of the clock

74298 Logic Schematic:



74373 (Latch)



Name: **74373** (Transparent Octal D-Type Latch With Output Enable)

Declaration: 74373(D1,D2,D3,D4,D5,D6,D7,D8,OEIN,G, OEON,Q8,Q7,Q6,Q5,Q4,Q3,Q2,Q1)

EPLDs: All

Default Signal Levels: GND — all input pins

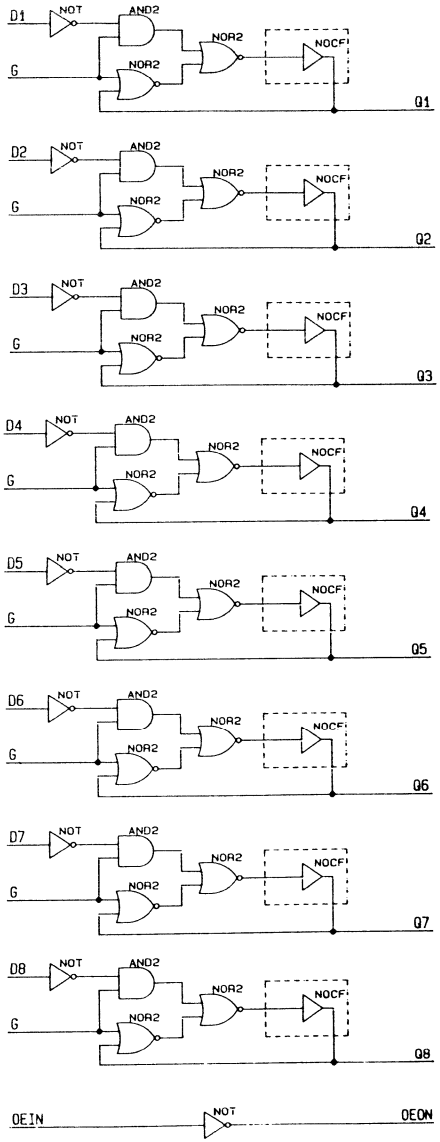
Function Table:

74373 Function Table

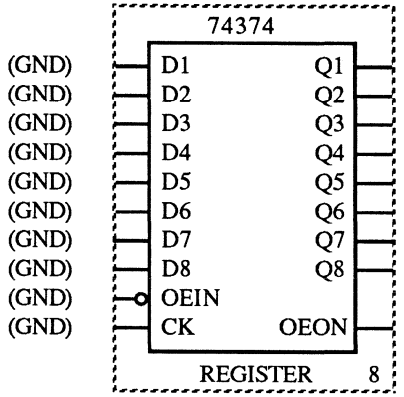
INPUTS			OUTPUTS	
OEIN	G	D	Q	OEON
L	X	X	X	H
H	X	X	X	L
X	H	L	L	X
X	H	H	H	X
X	L	X	Q_0	X

H = high level (steady state)
L = low level (steady state)
X = don't care
Q_0 = level of Q before the indicated steady-state input conditions were established

74373 Logic Schematic:



74374 (Register)



Name: **74374** (Octal D-Type Flip-Flop With Output Enable)

Declaration: 74374(D1,D2,D3,D4,D5,D6,D7,D8,OEIN, CK,OEON,Q8,Q7,Q6,Q5,Q4,Q3,Q2,Q1)

EPLDs: All

Default Signal Levels: GND — all input pins

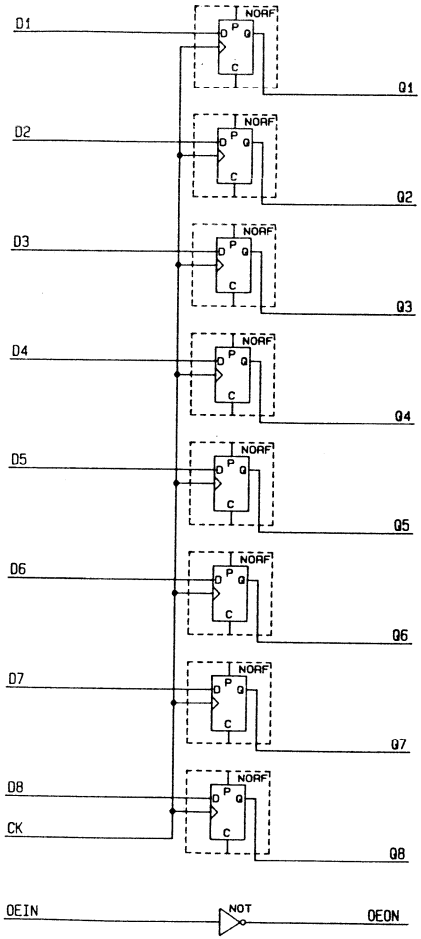
Function Table:

74374 Function Table

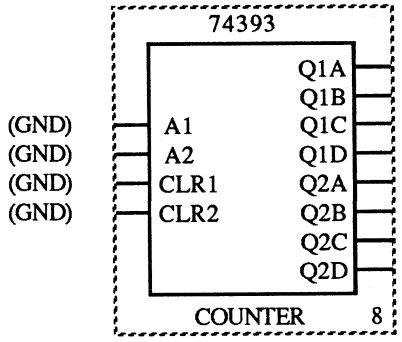
INPUTS			OUTPUTS	
CK	OEIN	D	Q	OEON
X	L	X	X	H
X	H	X	X	L
⌐	X	L	L	X
⌐	X	H	H	X
L	X	X	Q_0	X

H = high level (steady state)
L = low level (steady state)
X = don't care
Q_0 = level of Q before the indicated steady-state input conditions were established
⌐ = transition from low to high level

74374 Logic Schematic:



74393 (COUNTER)



Name: **74393** (4-Bit Up Counter With Asynchronous Clear)

Declaration: 74393(CLR1,CLR2,A1,A2,Q2D,Q2C,Q2B, Q2A,Q1D,Q1C,Q1B,Q1A)

EPLDs: EP600, EP610, EP900, EP910, EP1800, EPB1400

Default Signal Level: GND — all input pins

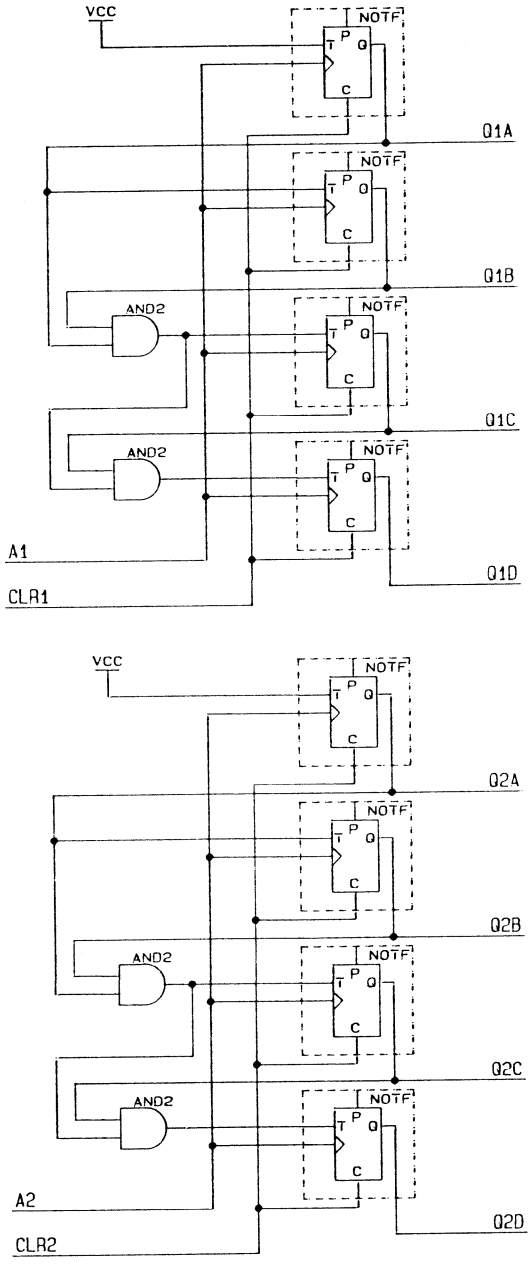
74393 Function Table:

74393 Function Table

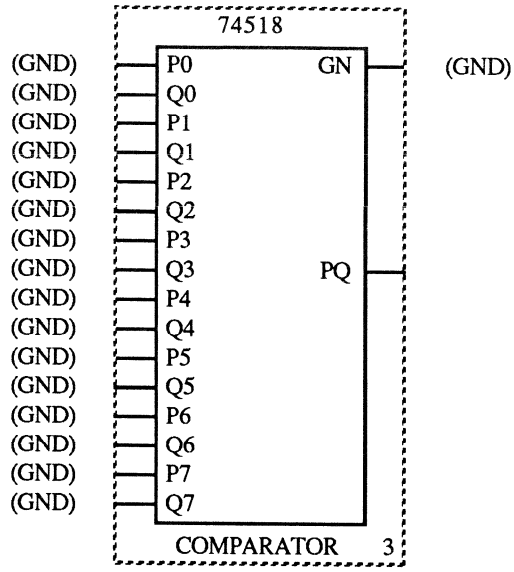
COUNT	INPUTS		OUTPUT			
	A	CLR	Q_D	Q_C	Q_B	Q_A
	X	H	L	L	L	L
0	⌐	L	L	L	L	L
1	⌐	L	L	L	L	H
2	⌐	L	L	L	H	L
3	⌐	L	L	L	H	H
4	⌐	L	L	H	L	L
5	⌐	L	L	H	L	H
6	⌐	L	L	H	H	L
7	⌐	L	L	H	H	H
8	⌐	L	H	L	L	L
9	⌐	L	H	L	L	H
10	⌐	L	H	L	H	L
11	⌐	L	H	L	H	H
12	⌐	L	H	H	L	L
13	⌐	L	H	H	L	H
14	⌐	L	H	H	H	L
15	⌐	L	H	H	H	H

H = high level
L = low level
⌐ = transition from low to high level

74393 Logic Schematic:



74518 (Comparator)



Name: **74518** (8-Bit Identity Comparator)

Declaration: 74518(P0,Q0,P1,Q1,P2,Q2,P3,Q3,P4, Q4,P5,Q5,P6,Q6,P7,Q7,GN,PQ)

EPLDs: EP600, EP610, EP900, EP910, EP1210, EP1800, EPB1400

Default Signal Levels: GND — all input pins

74518 Function Table:

74518 Function Table

INPUTS		OUTPUT	H = high level L = low level X = don't care
DATA P,Q	ENABLE GN	P = Q	
P=Q	L	H	
P>Q	L	L	
P<Q	L	L	
X	H	L	

74518 Logic Schematic: